Radiation-hard nanotechnology for space Systems-on-Chip

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ESA / ESTEC / Microelectronics Section

OVERVIEW

- European Space Agency overview
- Deep Sub-Micron Microchips: the brains of our satellites.
- Types of microchips: ASIC, FPGA, processors
- Smaller technology for bigger data
- Where are they used? How many? Costs?
- How are space microchips made?
- What can go wrong in space?
- Mitigating radiation effects
- ESA activity to have more and better space microchips
- One example: Space Multi-project Wafer Programme (180nm ASICs)
- Analogue and Mixed-signal microchips
- Silicon foundries and space DSM (180,65,28nm) libraries used for DSM SoCs
- Challenges ahead for space deep-submicron SoCs

ESA facts and figures

- Over 50 years of experience
- 22 Member States
- Eight sites/facilities in Europe, about 2200 staff
- 5.2 billion Euro budget (2016)
- Over 80 satellites designed, tested and operated in flight

European Space Agency

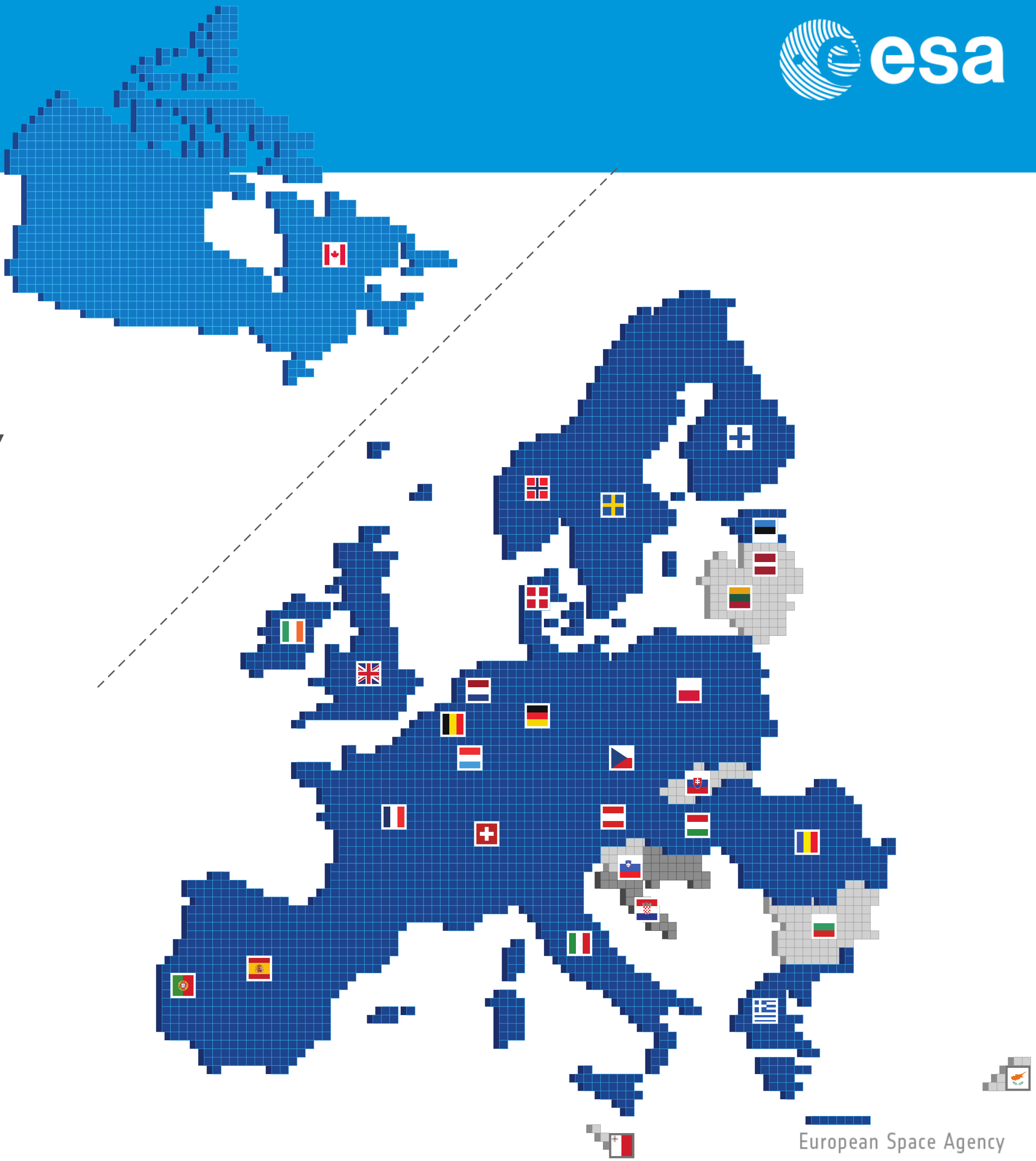
Purpose of ESA

“To provide for and promote, for exclusively peaceful purposes, cooperation among European states in **space research** and **technology** and their **space applications.**”

Article 2 of ESA Convention

European Space Agency

Member States

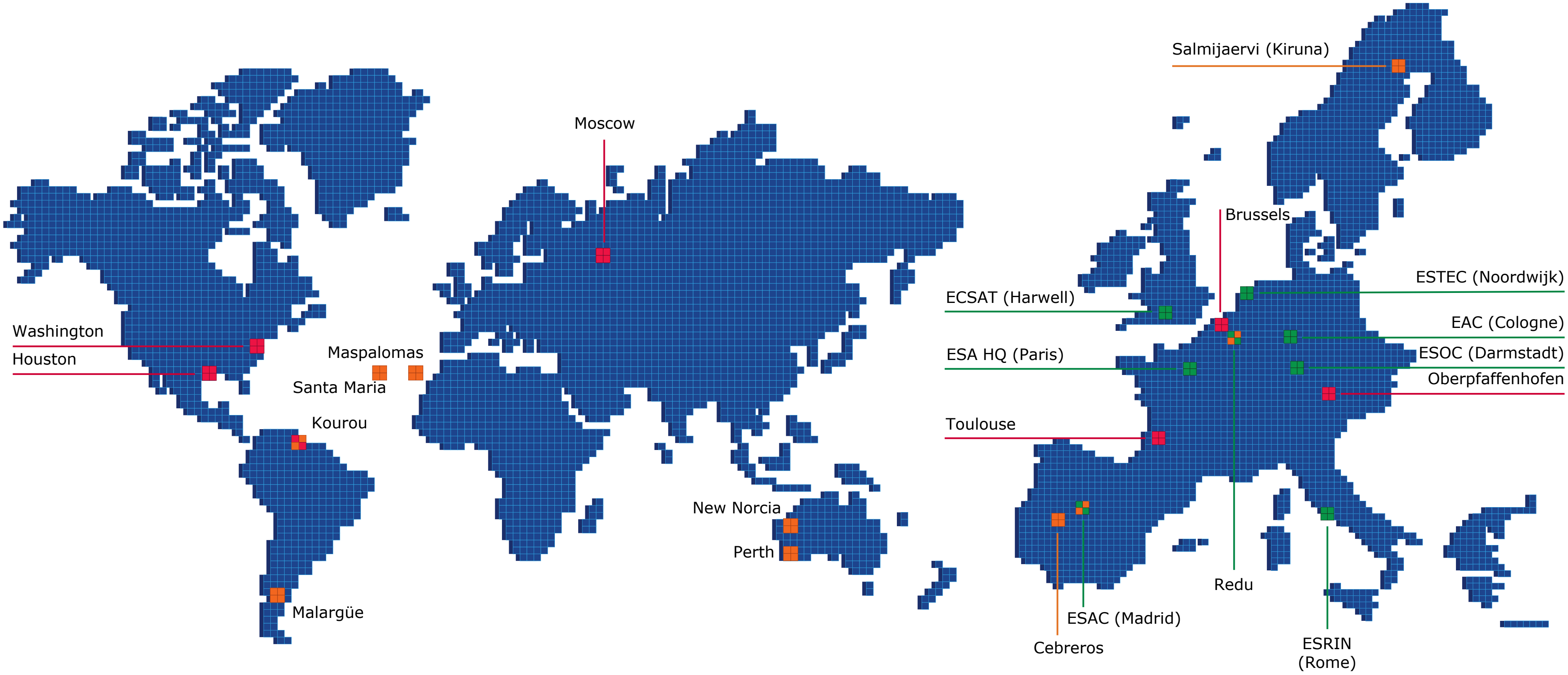


ESA has 22 Member States: 20 states of the EU (AT, BE, CZ, DE, DK, EE, ES, FI, FR, IT, GR, HU, IE, LU, NL, PT, PL, RO, SE, UK) plus Norway and Switzerland.

Seven other EU states have Cooperation Agreements with ESA: Bulgaria, Cyprus, Latvia, Lithuania, Malta, Slovakia and Slovenia. Discussions are ongoing with Croatia.

Canada takes part in some programmes under a long-standing Cooperation Agreement.

ESA’s locations



🟩 ESA sites

🟥 Offices

🟧 ESA Ground Station

▨ ESA Ground Station + Offices

▨ ESA sites + ESA Ground Station

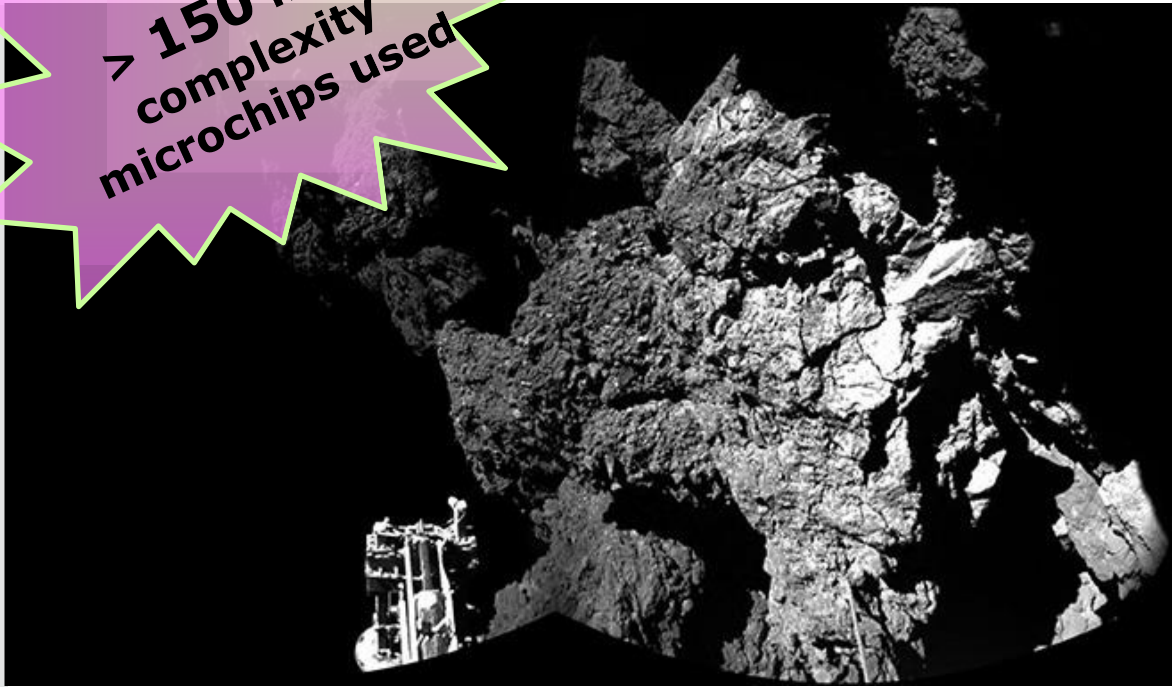
SCIENCE

Rosetta

First rendezvous, orbit and soft-landing on a comet.

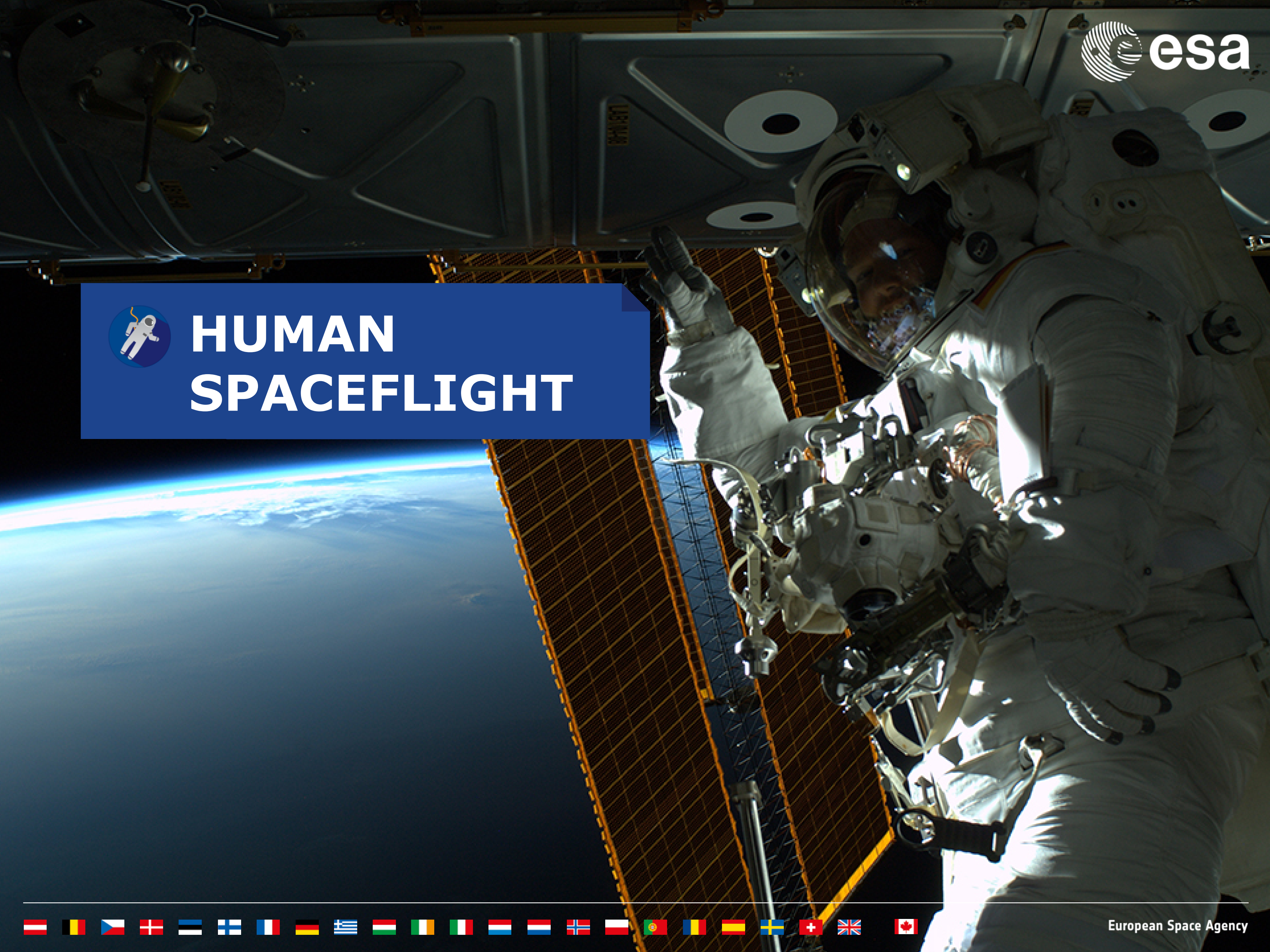
On 6 August 2014, ESA’s **Rosetta** became the first spacecraft to rendezvous with a comet 67P and, on 12 November, its Philae probe made the first soft-landing on a comet and returned data from the surface. The comet was **305 million km** from Earth, racing at **112464 km/h**.

Rosetta’s journey covered **6,4 billion km** and lasted **10 yrs**.

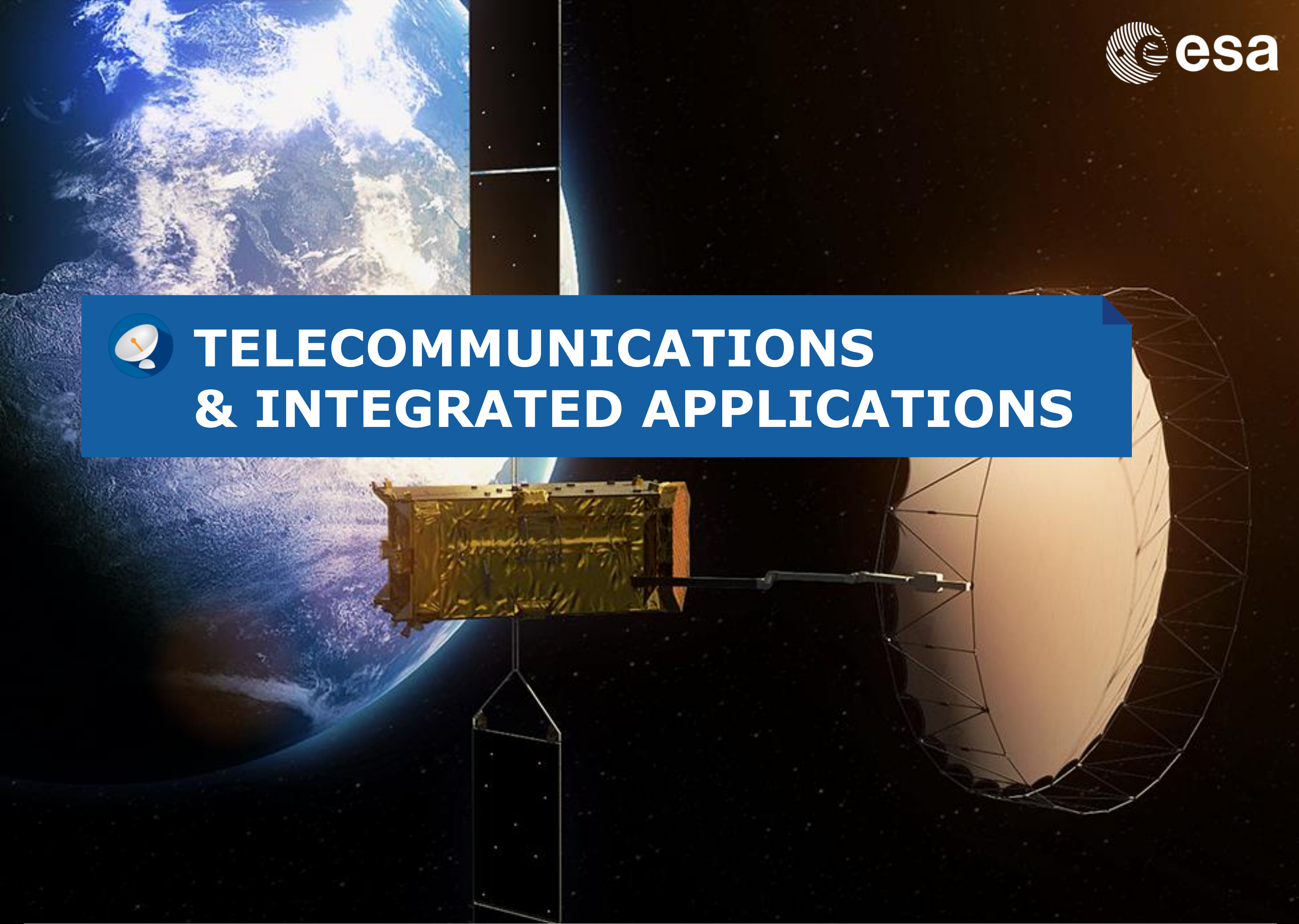


> 150 high complexity microchips used

NAVIGATION



HUMAN SPACEFLIGHT



TELECOMMUNICATIONS & INTEGRATED APPLICATIONS

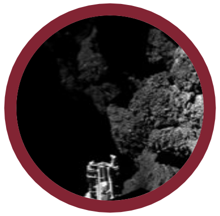
EARTH OBSERVATION

TECHNOLOGY

Activities

1.ESA is one of the few space agencies in the world to combine responsibility in nearly all areas of space activity.

* Space science is a Mandatory programme, all Member States contribute to it according to GNP. All other programmes are Optional, funded 'a la carte' by Participating States.


space science


human spaceflight


exploration


earth observation


launchers


navigation


operations


technology


telecommunications

European Space Agency

Missions

athena
Launch: 2028
Probing the hot and energetic Universe

plato
Launch: 2024
Hunting planets beyond our Solar System

juice
Launch: 2022
Europe's first mission to the Jupiter system

metop-sg series
Launch: 2021
MetOp Second Generation

euclid
Launch: 2020
Charting dark matter and dark energy's effects on the Universe

biomass
Launch: 2020
Measuring forest biomass

earthcare
Launch: 2018
Studying the roles of clouds and aerosols in our climate

james webb space telescope
Launch: 2018
Contributing two instruments to the next great space observatory

solar orbiter
Launch: 2018
Europe's closest mission to the Sun

mtg series
Launch: 2018
Meteosat Third Generation

european robotic arm
Launch: 2017
Robotic arm serving Russian segment of ISS

cheops
Launch: 2017
Studying planets around other stars

adm-aeolus
Launch: 2016
Mapping Earth's global wind fields

bepicolombo
Launch: 2016
Europe's first mission to Mercury

exomars
Launch: 2016, 2018
Mars orbiter and lander, followed by rover

lisa pathfinder
Launch: 2015
Technology demonstration for gravitational wave detection

smallgeo
Launch: 2015
New small platform for geostationary telecommunications

edrs
First launch: 2015
Geostationary satellites for relaying satellite data

ixv
Launch: 2015
Intermediate eXperimental Vehicle

alphasat
Launch: 2013
Innovative satellite telecommunications platform

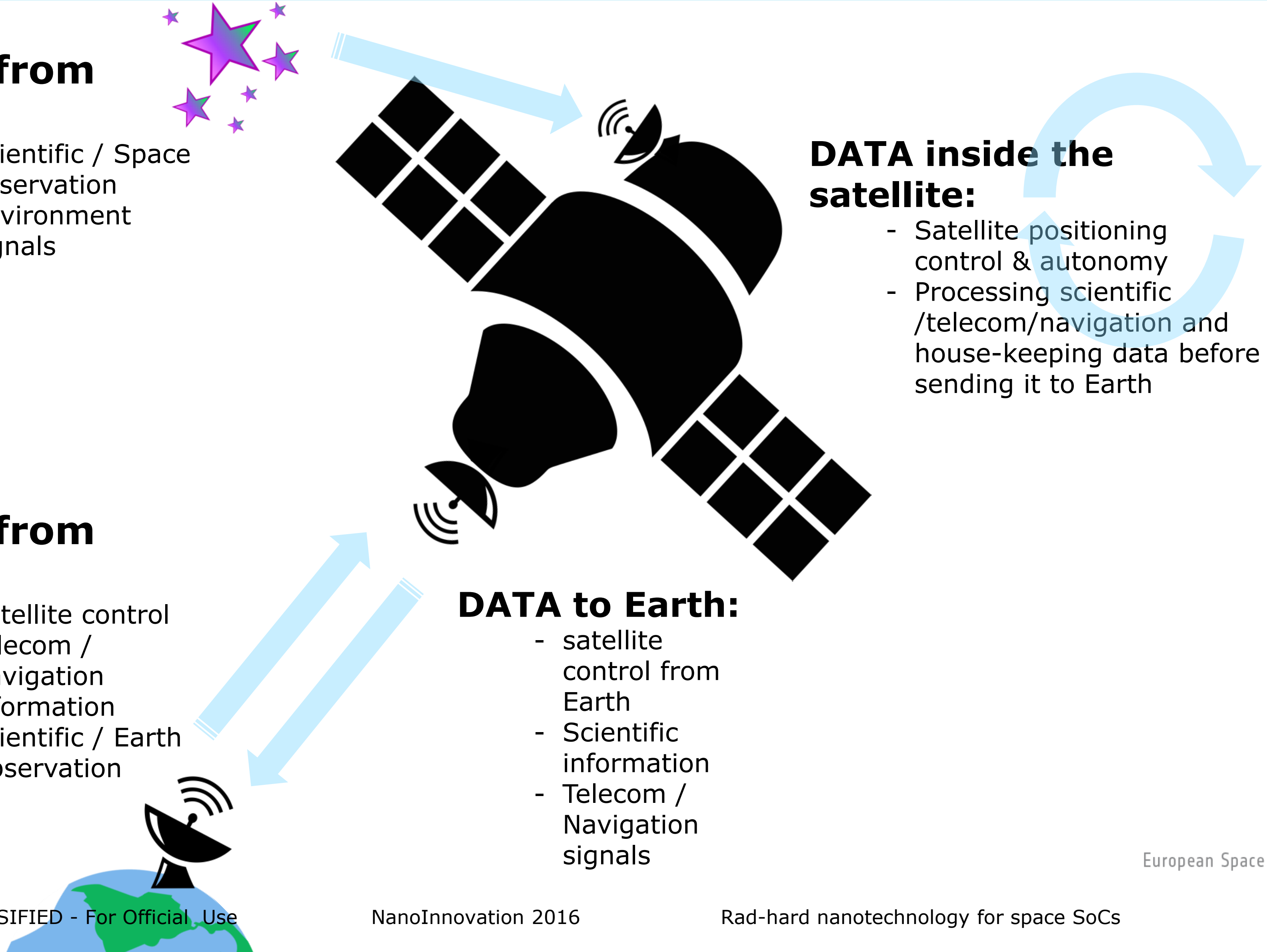
gaia
Launch: 2013
Mission to map a billion local stars in 3D

swarm
Launch: 2013
Trio of satellites mapping Earth's magnetic field

sentinel family
First launch: 2014
A portfolio of operational Earth observation missions

vega
First launch: 2012
Europe's small satellite launcher

How do our satellites handle all this data?



DATA from space:

- Scientific / Space observation
- Environment signals

DATA inside the satellite:

- Satellite positioning control & autonomy
- Processing scientific /telecom/navigation and house-keeping data before sending it to Earth

DATA from Earth:

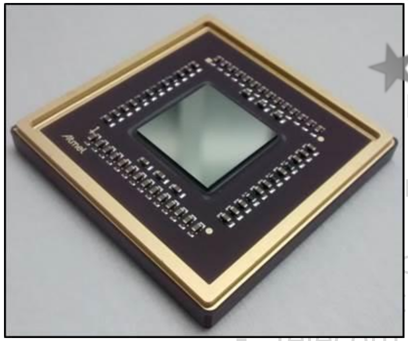
- Satellite control
- Telecom / Navigation information
- Scientific / Earth Observation

DATA to Earth:

- satellite control from Earth
- Scientific information
- Telecom / Navigation signals

The magic

Microchips: the brains "processing" the DATA



DATA from space:
- Scientific / Space observation
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DATA from Earth:
- Satellite control
- Telecom / Navigation information
- Scientific / Earth Observation

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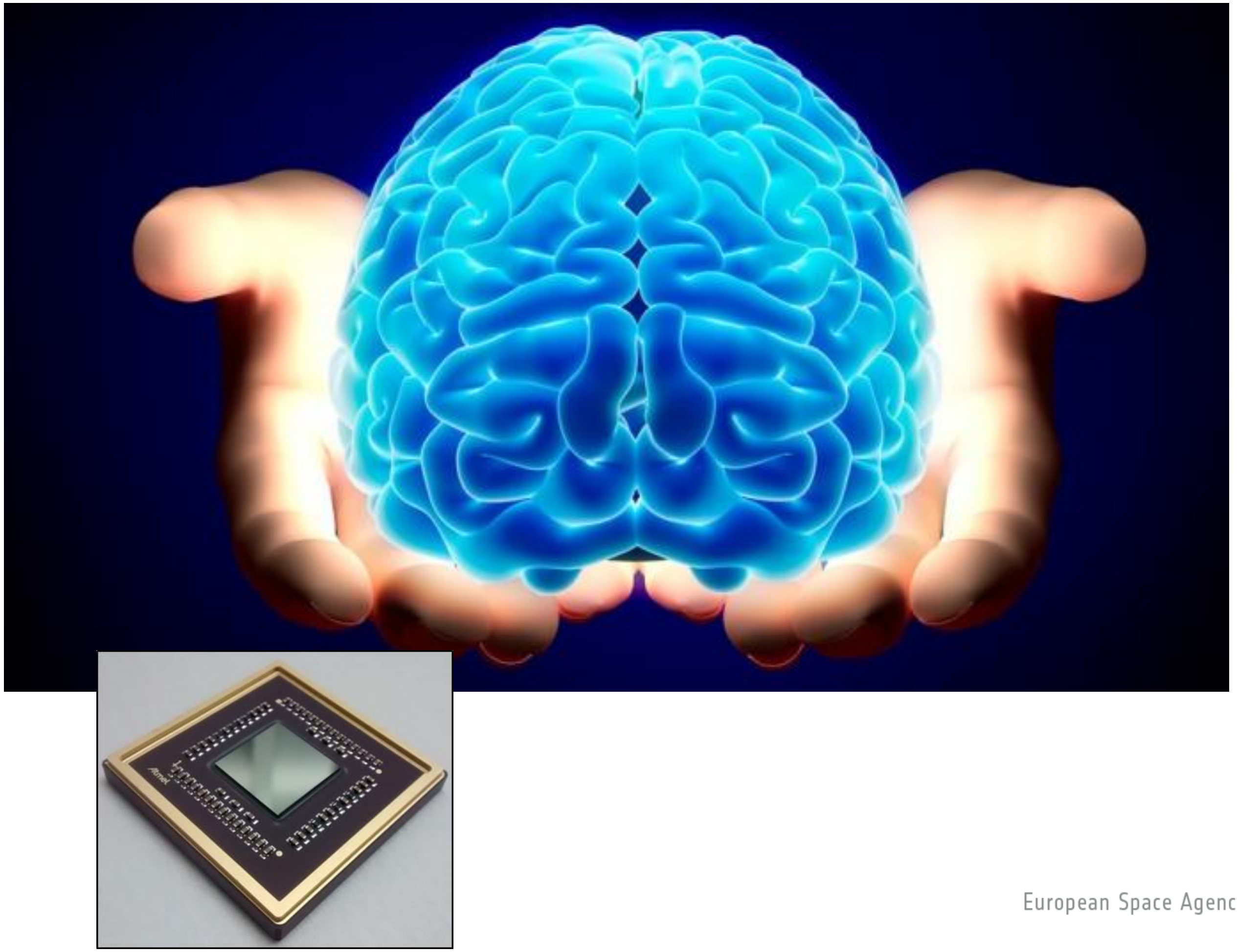
ion

- Telecom / Navigation signals

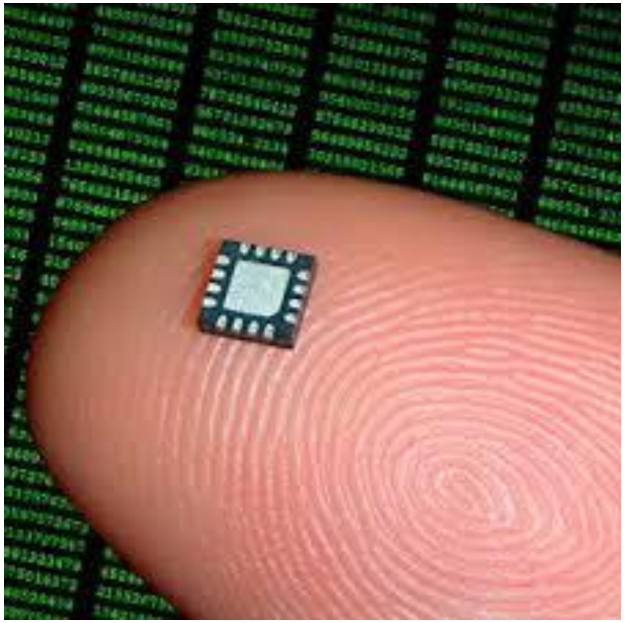
What do space Microchips do with the DATA?

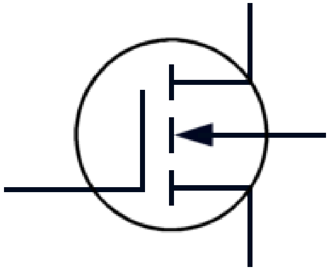
- Receive
- Select
- Compare
- Calculate
- Decide
- Compress
- Authenticate
- Monitor
- Wait
- Store
- Send
- Activate
- Stop
- …

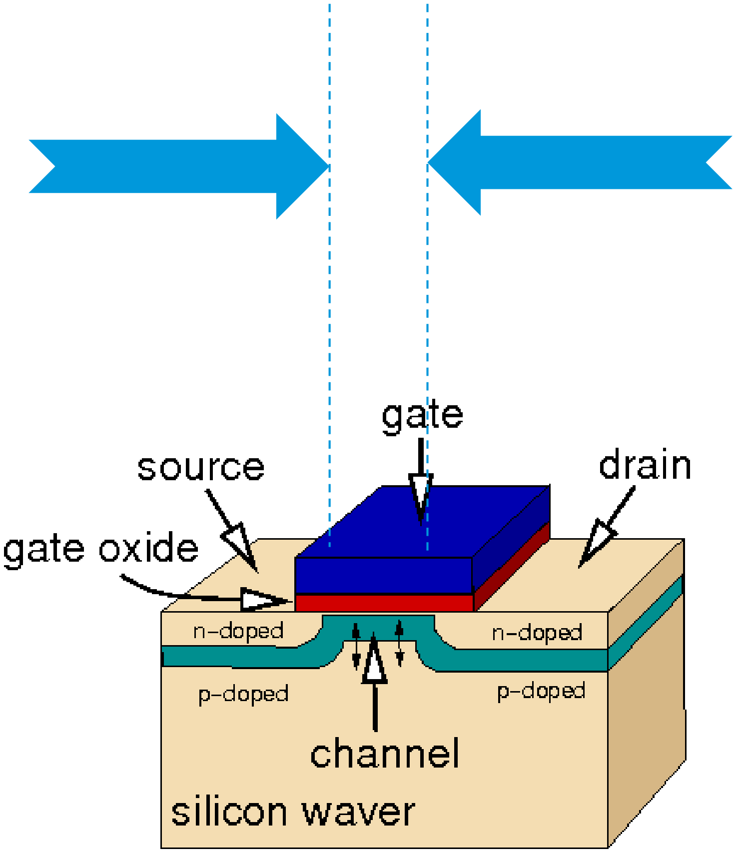


what is a “deep submicron” microchip?

integrated circuit smallest “feature size” (i.e. “**transistor gate length**”) measures far less than 1µm, that is **180nm, 65nm, 28nm, or smaller size** ....







Metal–Oxide Field–Effect Transistor (MOSFET)

Types of deep sub-micron space microchips

ASIC

Application Specific Integrated Circuits

- Reused locally by developing companies
- some available to the open market (ASSPs*)

FIXED SPECIALISED FUNCTIONS (some embed microprocessor cores) / best performances / Digital, Analogue and Mixed-signal

FPGA

Field Programmable Gate Arrays

ONE-TIME, LIMITED or UNLIMITED REPROGRAMABLE to decide FUNCTIONS / easier/cheaper to change

- Generic use
- Off-the-shelf products for the open market

Microprocessors

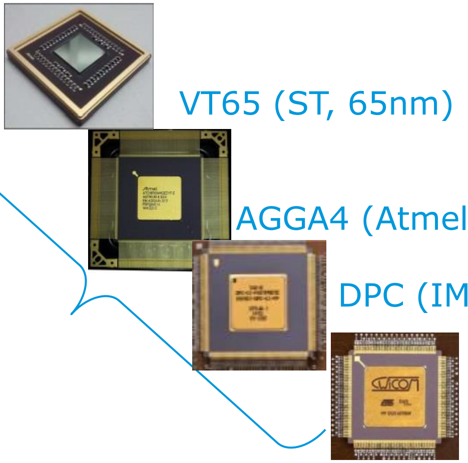
Use SOFTWARE stored in external memories to implement FUNCTIONS

* ASSP = Application Specific Standard Product

Recent European sub-micron space microchips

ASIC

Application Specific Integrated Circuits



VT65 (ST, 65nm) 2015

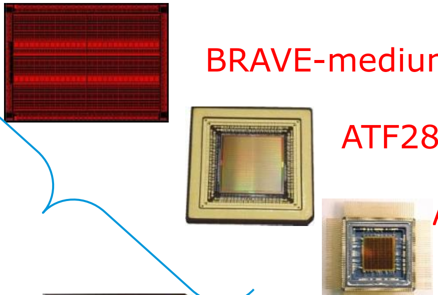
AGGA4 (Atmel, 180nm) 2015

DPC (IMEC, 180nm) 2015

CWICOM
(Atmel, 180nm) 2012

FPGA

Field Programmable Gate Arrays

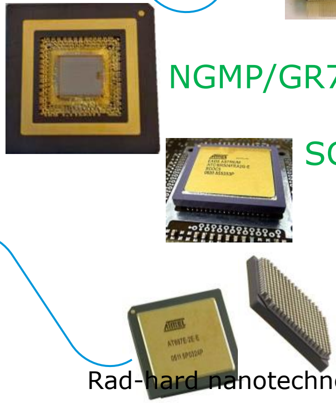


BRAVE-medium (ST, 65nm) 2016

ATF280F (Atmel, 180nm) 2009

AT40K (Atmel, 350nm) 2004

Microprocessors



NGMP/GR740 (ST, 65nm) 2015

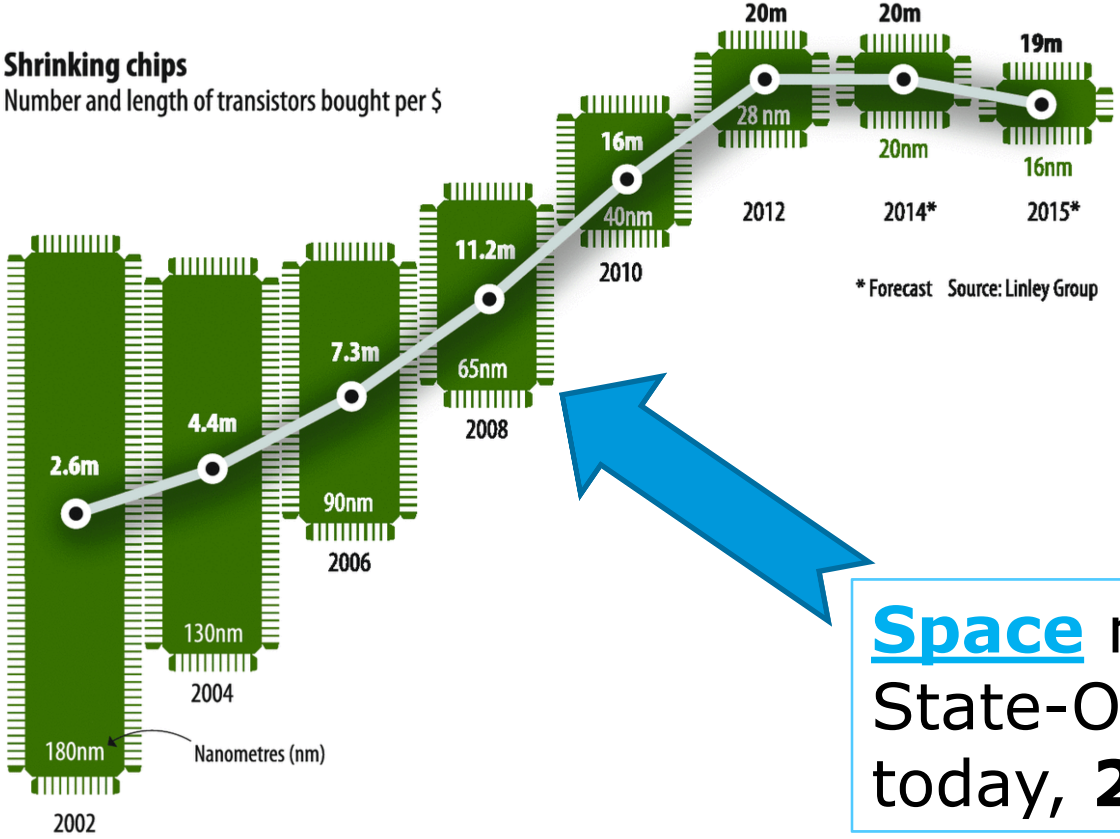
SCOC3 (Atmel, 180nm) 2008

AT697 LEON2FT (Atmel, 180nm)
2005

Commercial vs space microchips

Smaller means **faster, less power, lighter equipment**, but also **more expensive and complex to develop**

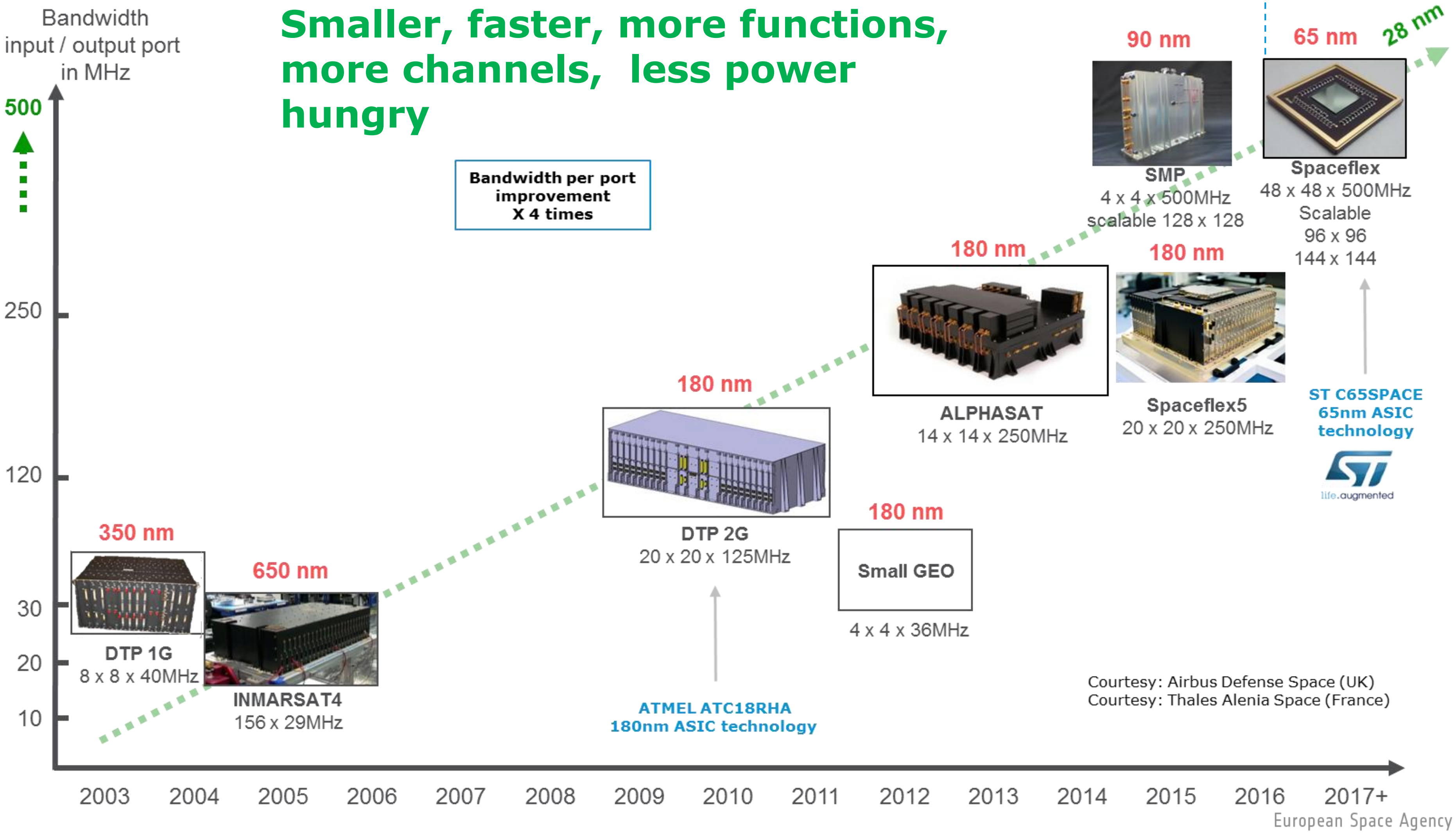
Commercial Technology



Space microchip State-Of-The-Art today, **2016**!!

Digital Telecom processors improve with DSM Microchips

Smaller, faster, more functions, more channels, less power hungry



Bandwidth per port improvement X 4 times

350 nm
DTP 1G
8 x 8 x 40MHz

650 nm
INMARSAT4
156 x 29MHz

180 nm
DTP 2G
20 x 20 x 125MHz

ATMEL ATC18RHA 180nm ASIC technology

180 nm
Small GEO
4 x 4 x 36MHz

180 nm
ALPHASAT
14 x 14 x 250MHz

90 nm
SMP
4 x 4 x 500MHz
scalable 128 x 128

180 nm
Spaceflex5
20 x 20 x 250MHz

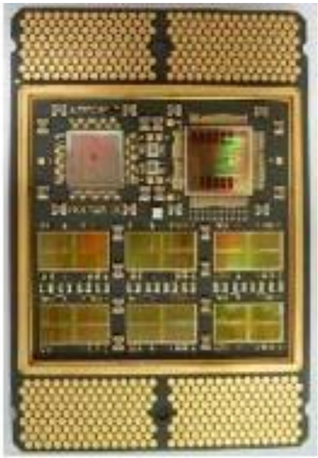
65 nm
Spaceflex
48 x 48 x 500MHz
Scalable
96 x 96
144 x 144

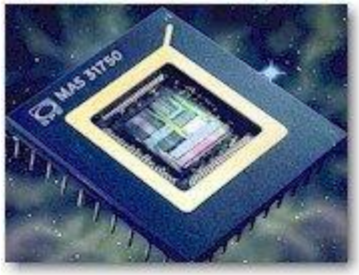
ST C65SPACE 65nm ASIC technology

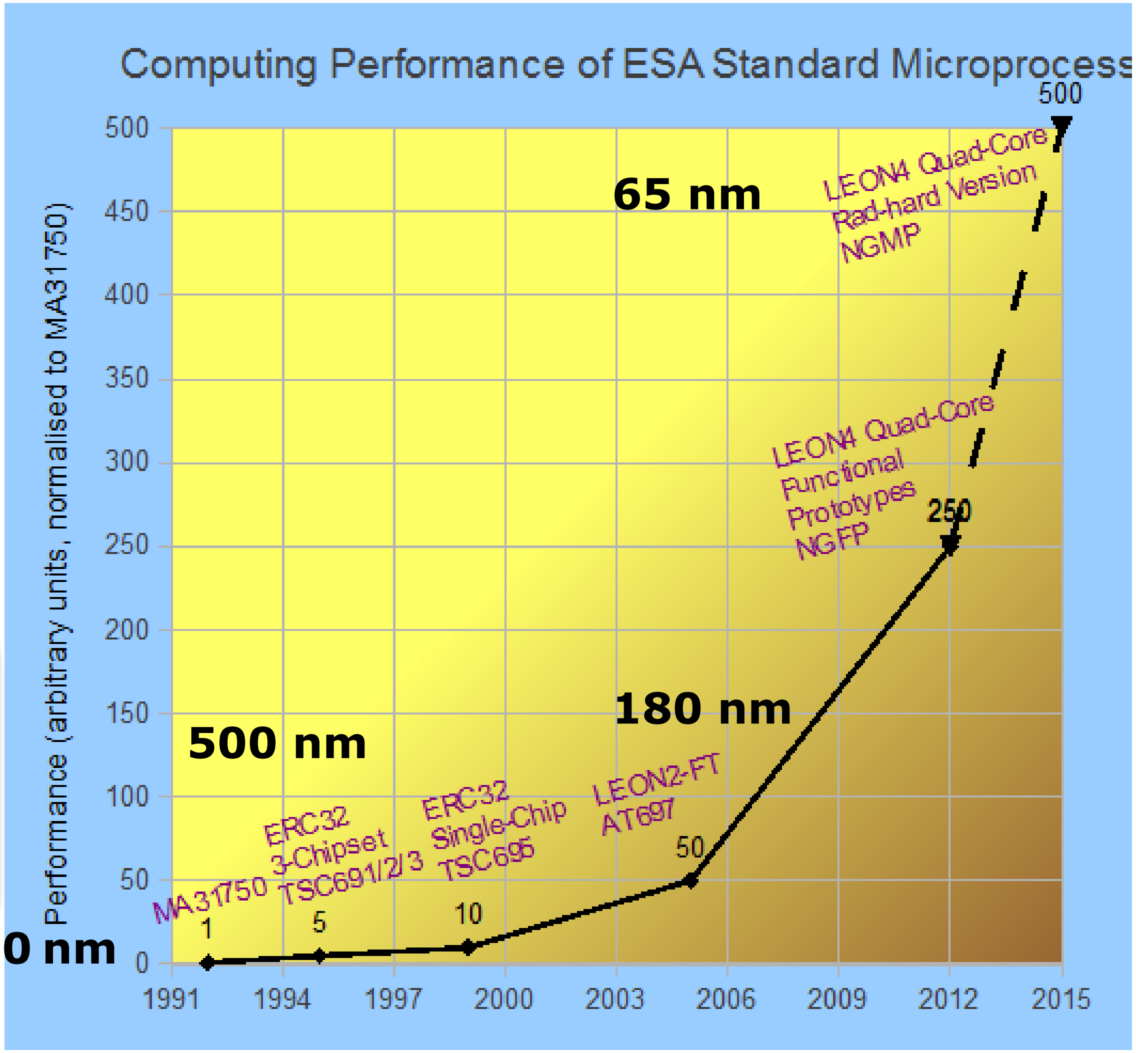
life.augmented

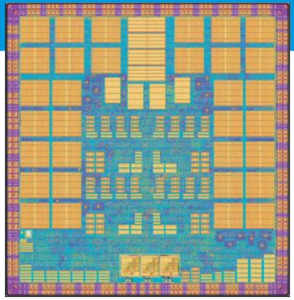
Courtesy: Airbus Defense Space (UK)
Courtesy: Thales Alenia Space (France)

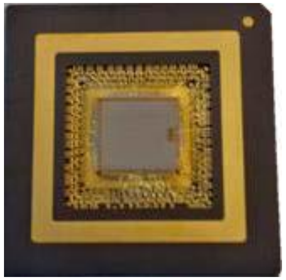
Microprocessors: better performance thanks to DSM technology

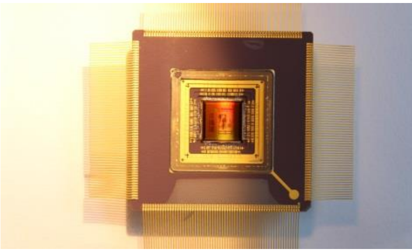




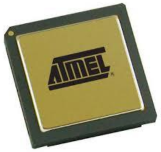








Components for Satellite Data-Handling - Processor



TSC695

500nm RTP CMOS
TID 300krad
SEL 80 MeVcm2/mg

PROCESSOR	SPARCv7
SPEED	25MHz
PROCESSING	20MIPS
PROM/SRAM I/F	

- FPU
- GPT
- RTCT
- UART 2x
- RAM I/F

AT697

180nm ATC18RHA CMOS
TID 300krad
SEL >60 MeVcm2/mg

PROESSOR	SPARCv8/LEON2
SPEED	100MHz
MIPS	86MIPS
I-CACHE	32kbyte
D-CACHE	16kbyte
PROM/SRAM/SDRAM I/F	

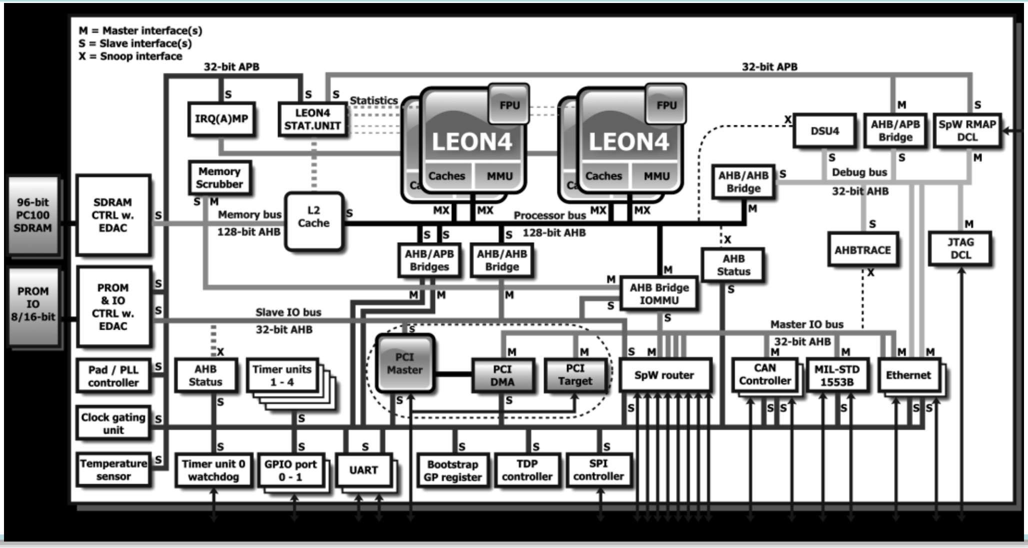
- PCI
- GPIO
- UART 2x
- TMR

NGMP

ST 65nm CMOS
TID 300krad
SEL >60 MeVcm2/mg

PROCESSOR	LEON4 4x
SPEED	250MHz
PROCESSING	900MIPS
Cache	L1
Cache	L2
SDRAM/PROM I/F	

- PCI
- ETH
- SpW 8x
- CAN 2x
- 1553
- SPI
- GPIO
- TMR



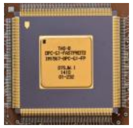
Components for Satellite Data-Handling - Microcontroller

80C32

800nm RT CMOS
TID 30krad
SEL 80 MeVcm2/mg

PROCESSOR	8 bit
SPEED	30MHz
RAM	256byte
OSC	

UART
RAM I/F
TMR



DPC

DARE 180nm CMOS
TID 100krad
SEL 60 MeVcm2/mg

PROCESSOR	16 bit
SPEED	40MHz
RAM	42kbyte
PROM I/F	

ADC 12b 1MSps 4x
DAC 12b 3MSps 3x
PWM 6x
1553
CAN 2x
UART 3x

MESA

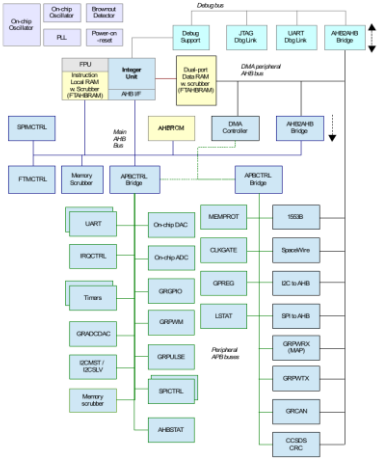
DARE 180nm CMOS
TID 100krad
SEL 60 MeVcm2/mg

PROCESSOR	32bit LEON2
INSTR SET	16/32 bit
SPEED	50MHz
RAM	

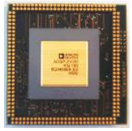
ADC 10b 100kSps
DAC 10b 100kSps
OSC

1553
CAN
SpW
SPI 2x
I2C
ADC/ I/F
DAC I/F

PWM
TMR
GPIO
RAM I/F



Components for Satellite Data-Handling - DSP



TSC21020

600nm RTP CMOS
TID 100krad
SEL 80 MeVcm2/mg

PROCESSOR	32/40 bit VLIW	PROM I/F
SPEED	20MHz	RAM I/F
PROCESSING	40MOps	
1024pt FFT	975us	
MAC (float))	50ns	

SSDP

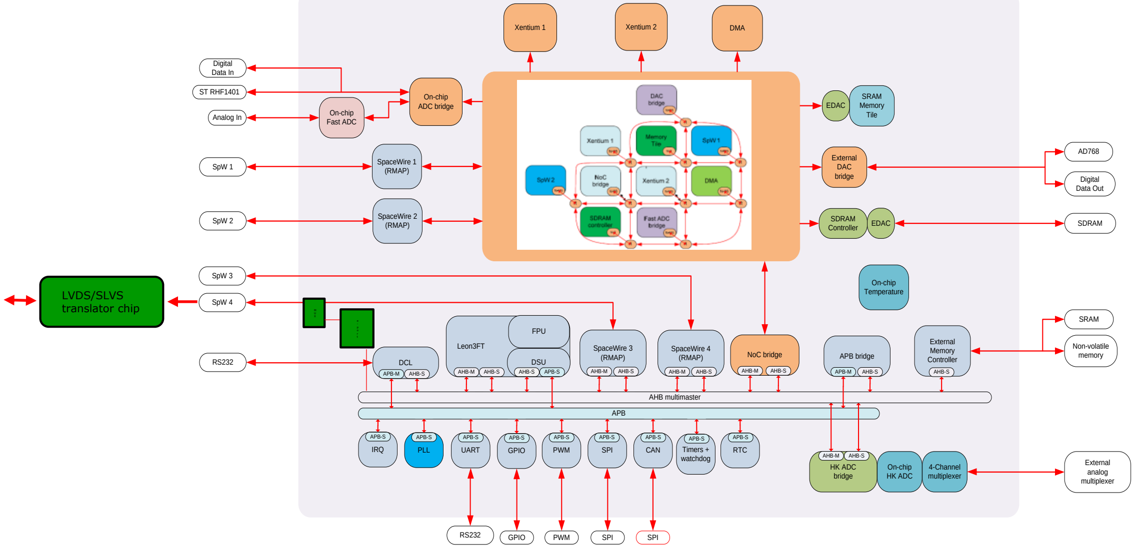
DARE 180nm CMOS
TID 1000krad
SEL 60 MeVcm2/mg

PROCEESOR1	LEON2
SPEED	100MHz
PROCEESOR2	VLIW
SPEED	100MHz
PROCESSING	1000MOsp
1024pt FFT	24us
MAC (32bit)	2.5ns

PROM I/F
RAM I/F

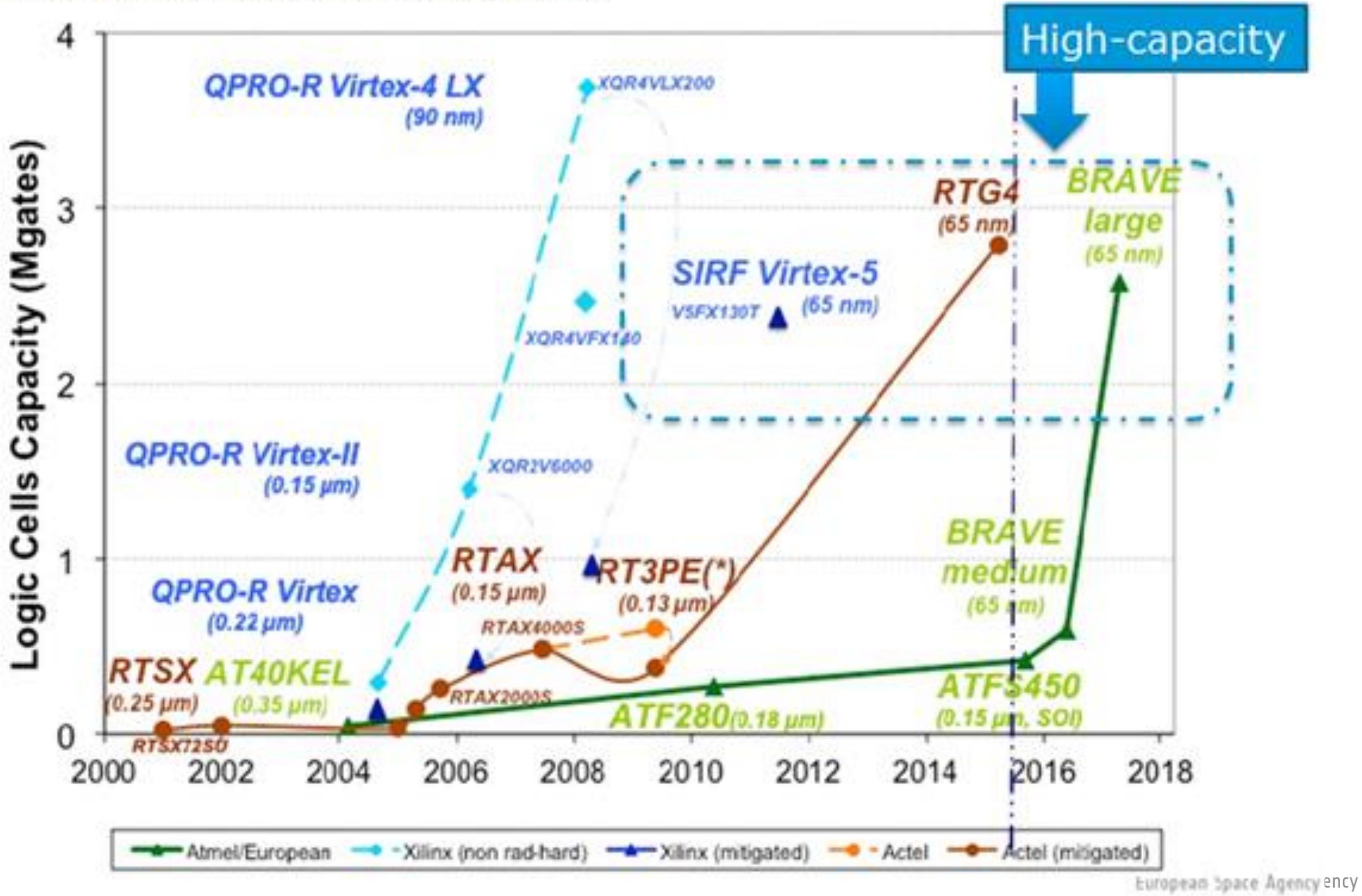
ADC 12b 1MSps
ADC 10b 100MSps

CAN 2x
SpW 4x
SPI 2x
PWM
GPIO
UART
ADC/DAC-IF



FPGAs: better performance and functional capacity thanks to DSM technology

Note: RTG4, ATFS450 and BRAVE dates are for Engineering Samples



BRAVE: the new European reprogrammable space FPGA

NG-FPGA-MEDIUM Characteristics

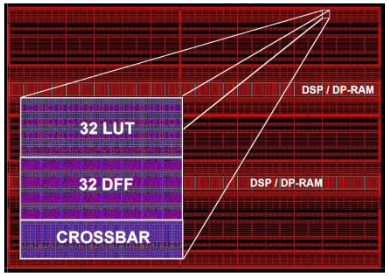
☐Power supply
- Core: 1,2V ±10%
- IOS: 1.5V ±10% or 1.8V ±10% or 2.5V ±10% or 3.3V ±10%

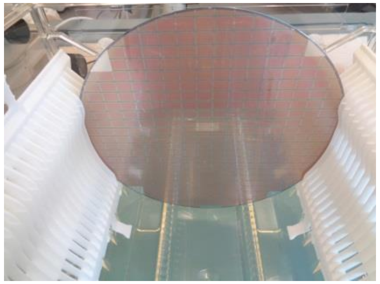
☐Performance
- 250MHz Logic
- 333MHz DSP
- 800Mbps I/O

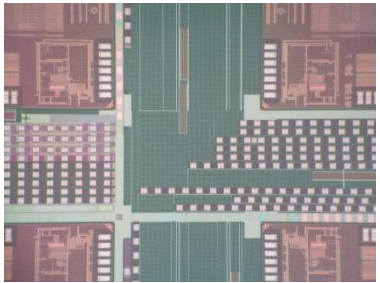
☐Temperature
- -55ºC to +125ºC

☐ESD
- HBM > 2000V for all IOB, Control IO and power supplies

Device	NG-MEDIUM
Capacity	
Equivalent System Gates	4 400 000
ASIC Gates	550 000
Modules	
Register	32 256
LUT-4	34 272
Carry	8 064
Embedded RAM	
Core RAM Blocks (48K-bits)	56
Core RAM Bits (K = 1024)	2688 K
Core Register File (64 x 16-bits)	168
Core Register File Bits	168 K
Embedded DSP	112
Clocks	32
Embedded Serial Link	
SpaceWire 400Mbps	1
I/Os	
I/O Banks	13
User I/Os	
LGA-625	390
MQFP-352	208
I/O PHY	
DDR	16
SpaceWire	16



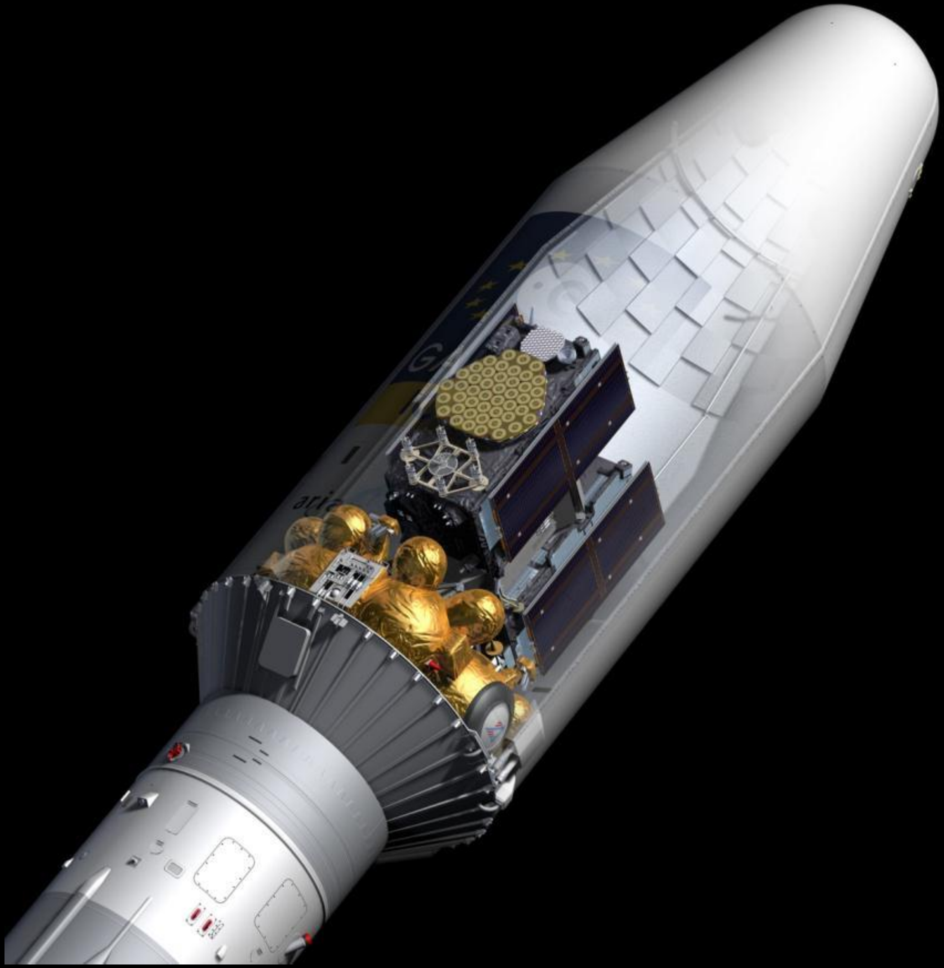




NG-MEDIUM in 2016
NG-LARGE in 2017
NG-ULTRA in 2018

For more information contact Edouard Lepape: elepape@nanoxplore.com

Spacecraft Sub-Systems: where are the microchips?



PLATFORM

Structures
Power
Thermal Control
Attitude Control
Guidance
Command and Data Handling
Propulsion
Harness

PAYLOAD Instruments

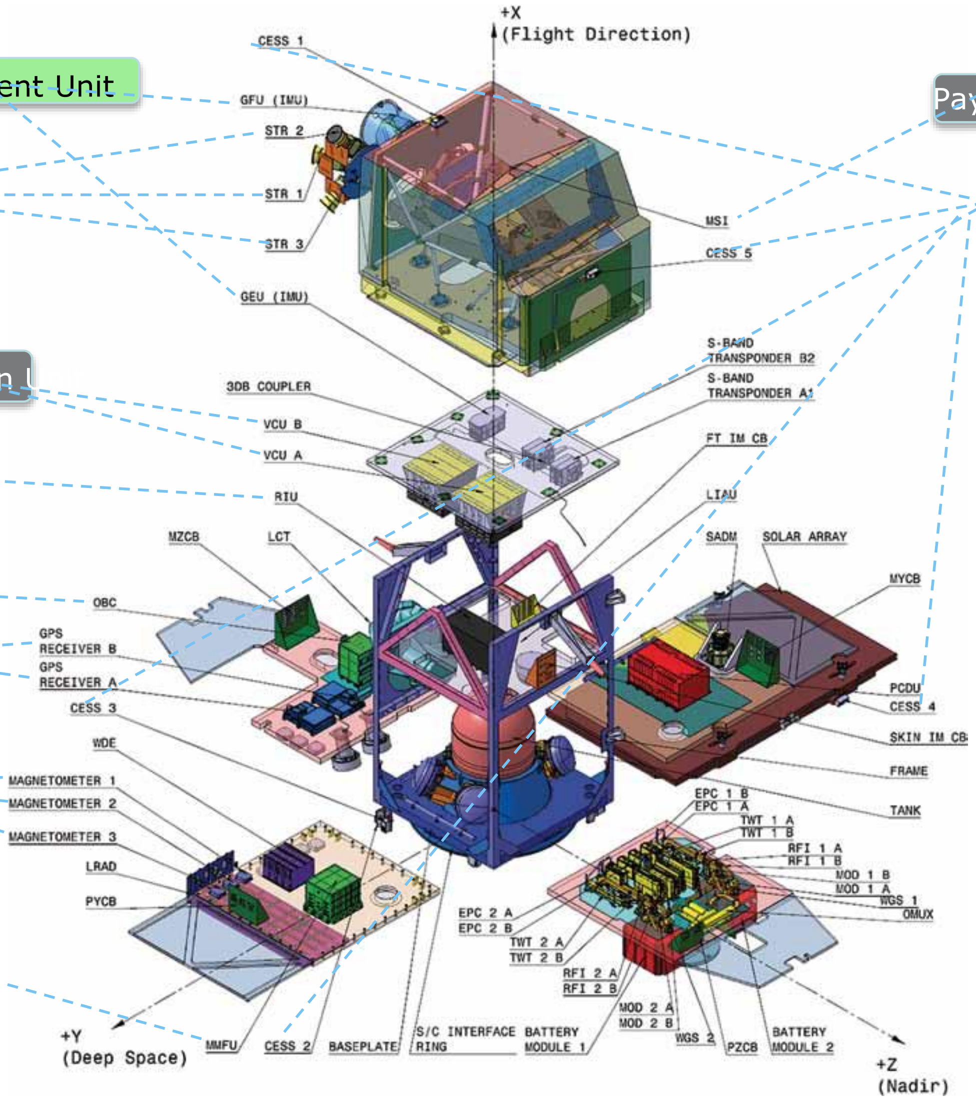
Life Support

Launcher

Ground Segment

Deconstructing a Spacecraft to Component Level: Sentinel-2

Deconstructing a Spacecraft to Component Level: Sentinel-2



Sensor – Inertial Measurement Unit

Sensor – Star Tracker

Payload – Video Compression U

Remote Interface Unit

On Board Computer

Sensor – GPS

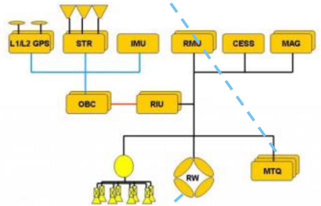
Sensor – Magnetometer

Mass Memory

Payload – Multi Spectral Imager

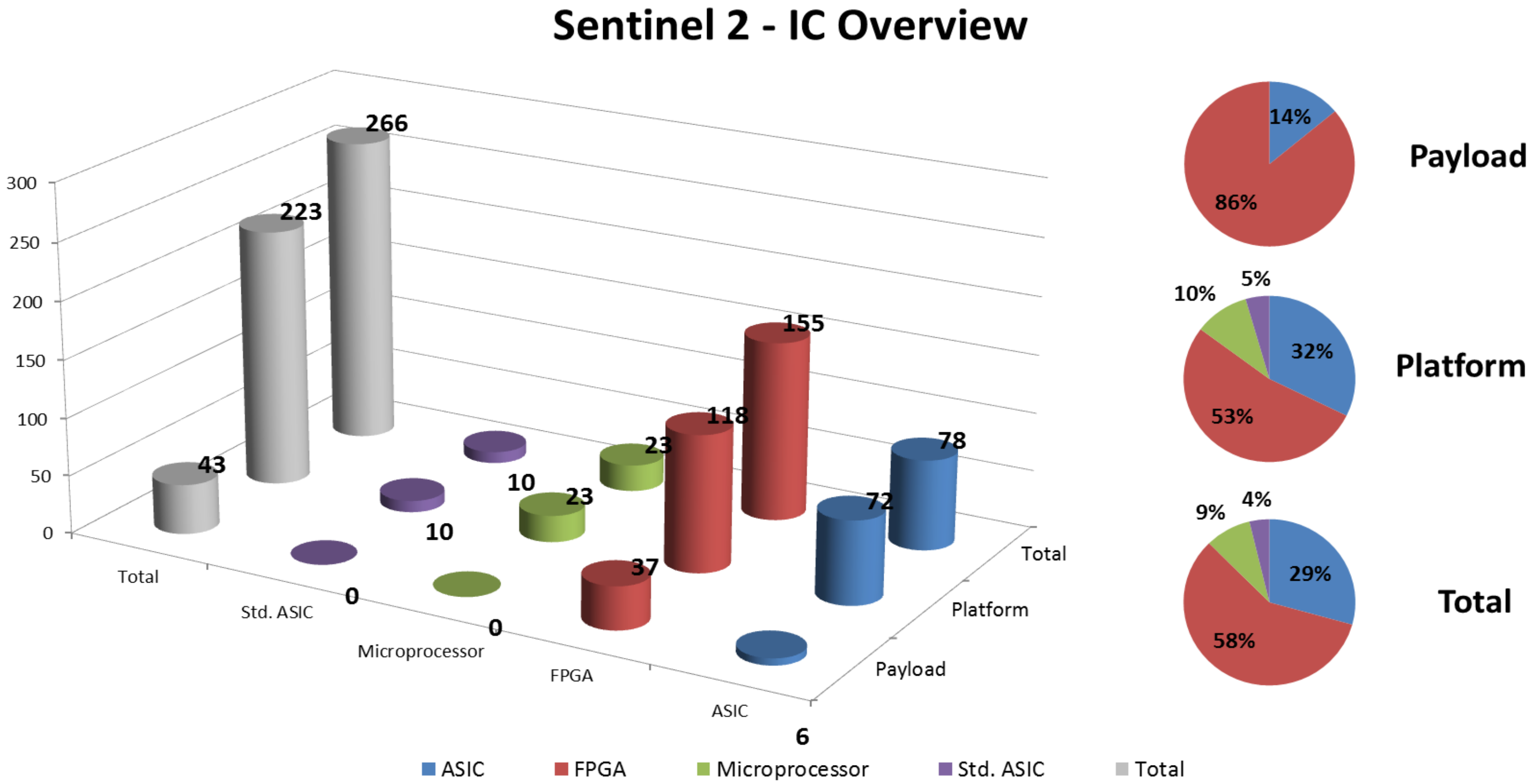
Sensor – Coarse Earth/Sun Sensor

Actuator– Magneto Torque



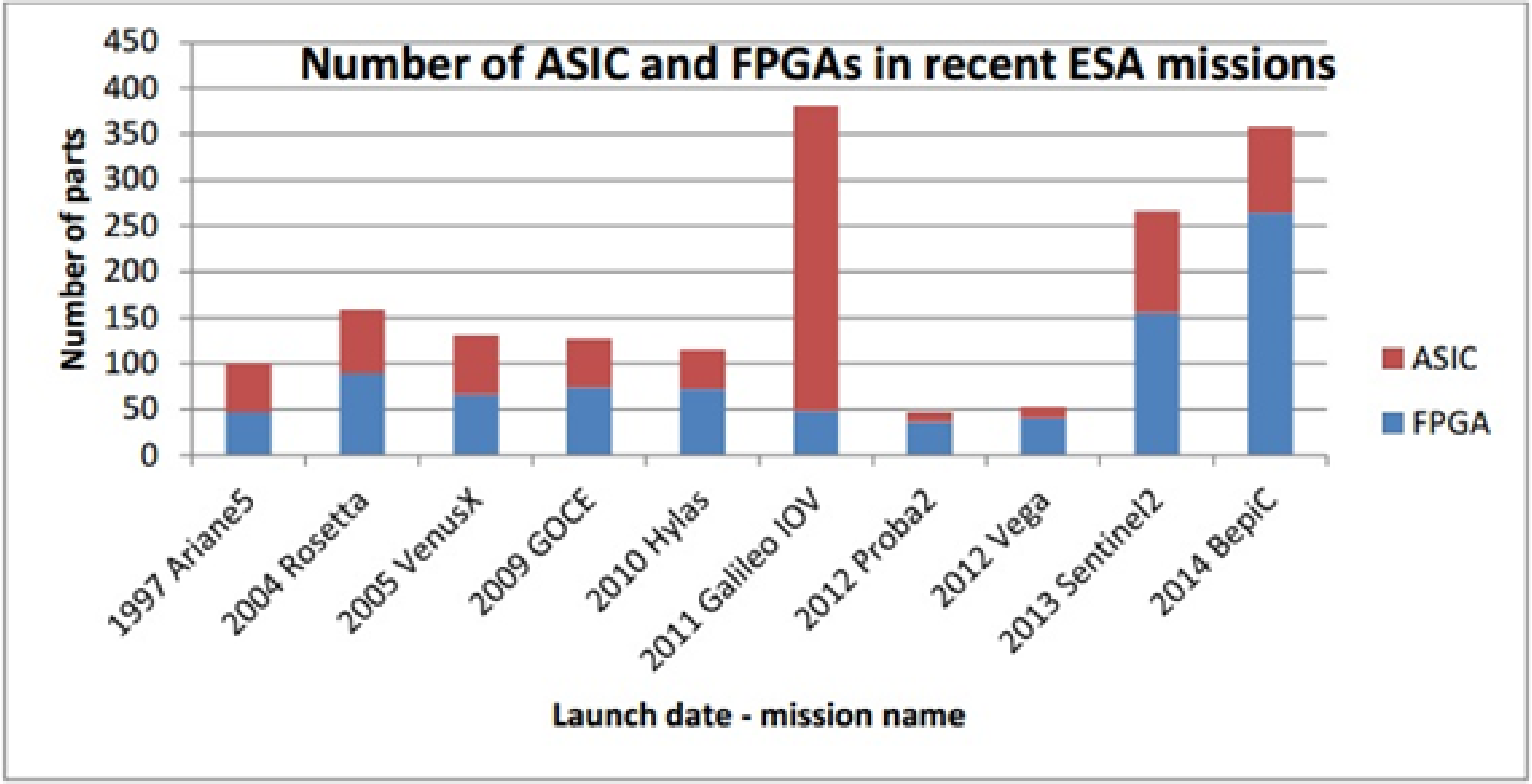
Actuator – Reaction Wheel

SENTINEL 2 : ASICs and FPGAs used



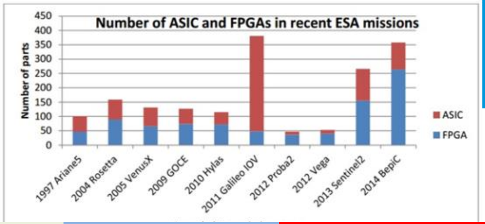
- Sentinel 2 uses 266 complex ICs (excluding imagers and sensors) out of which around 85% of them are used in the platform and only a 15% in the payload

How many complex microchips in our satellites?



Trends and patterns of ASIC and FPGA use in European space missions; ESA/TU Delft, April 2013; https://amstel.estec.esa.int/tecedm/website/stag_ygt/Boada.pdf

How much money is spent in microchips per satellite?



Number of ASICs and FPGAs procured per satellite		**FPGA**	**ASIC (0.5-0.18um)**	**TOTAL**
	TOTALs (10yrs, 10 missions)	875	805	1680
	Average per mission (10yrs, 10 missions)	**87.5**	**80.5**	**168**
Prices per device (rough estimates)				
	Lowest price per device	5K€	15K€	
	Highest price per device	40K€	80K€	
	Averaged price per device	**22K€**	**47K€**	
Average rough estimate expenditure per mission on complex microchips (10yrs, 10 missions) (NRE costs, design and technology predevelopments NOT INCLUDED; just the price per device!)		**2M€**	**3,8M€**	**5,8M€**

Trends and patterns of ASIC and FPGA use in European space missions; ESA/TU Delft, April 2013; https://amstel.estec.esa.int/tecedm/website/stag_ygt/Boada.pdf

How are deep sub-micron space microchips created?

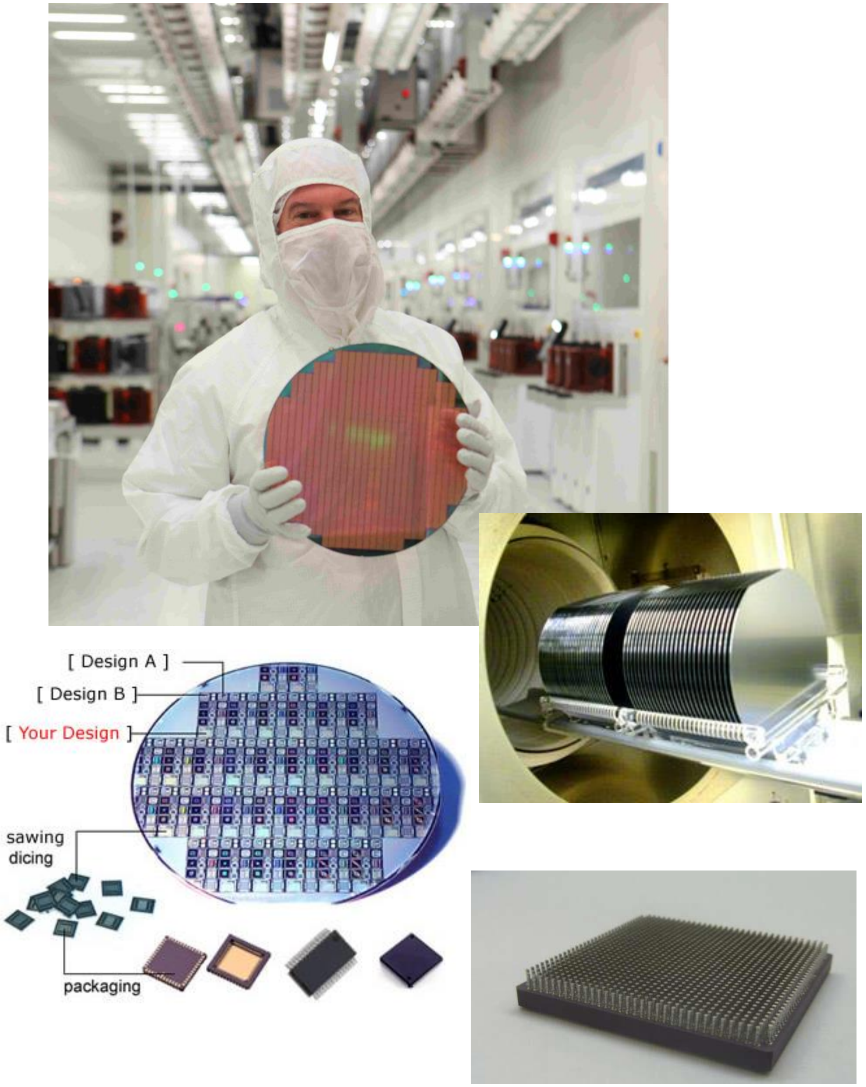
✓ **silicon wafer foundries** using reliable (few defects, long life time, working in space extreme T) "**Deep-submicron**" manufacturing processes **STMicrolectronics, UMC(Taiwan), Xfab(Malaysia), etc.**

✓ **Radiation hard** basic IC building blocks => "**Rad-hard ASIC libraries" and "IP cores"**,

ST-C65SPACE, Microchip Atmel-ATMX150RHA, IMEC-DARE, etc.

✓ Space qualified chip **package technology** **E2V, HCM**

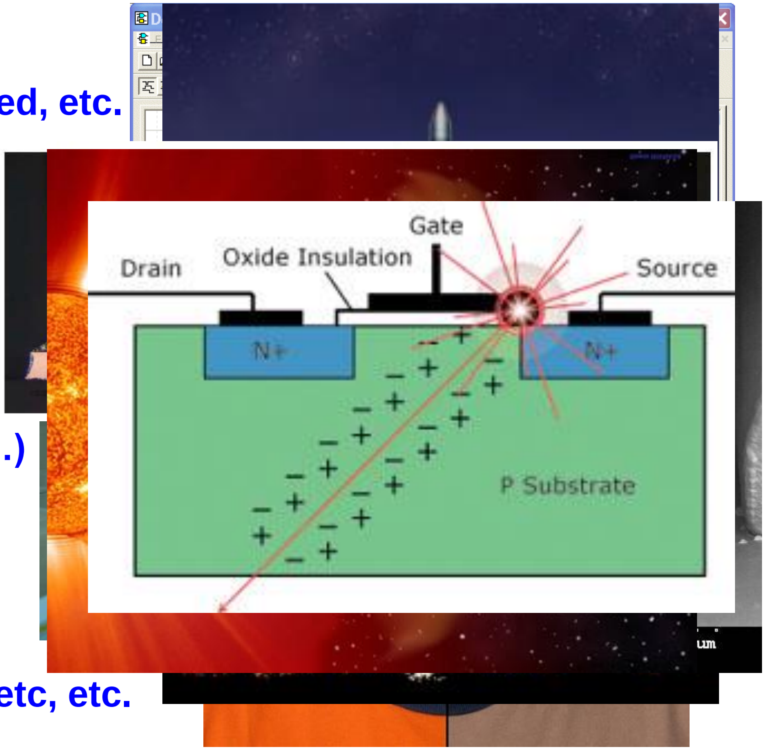
✓ **Space quality control** of the whole supply chain **ST, Microchip Atmel, IMEC, Cobham…**



Manufacturing microchips… in 1.5 minutes!

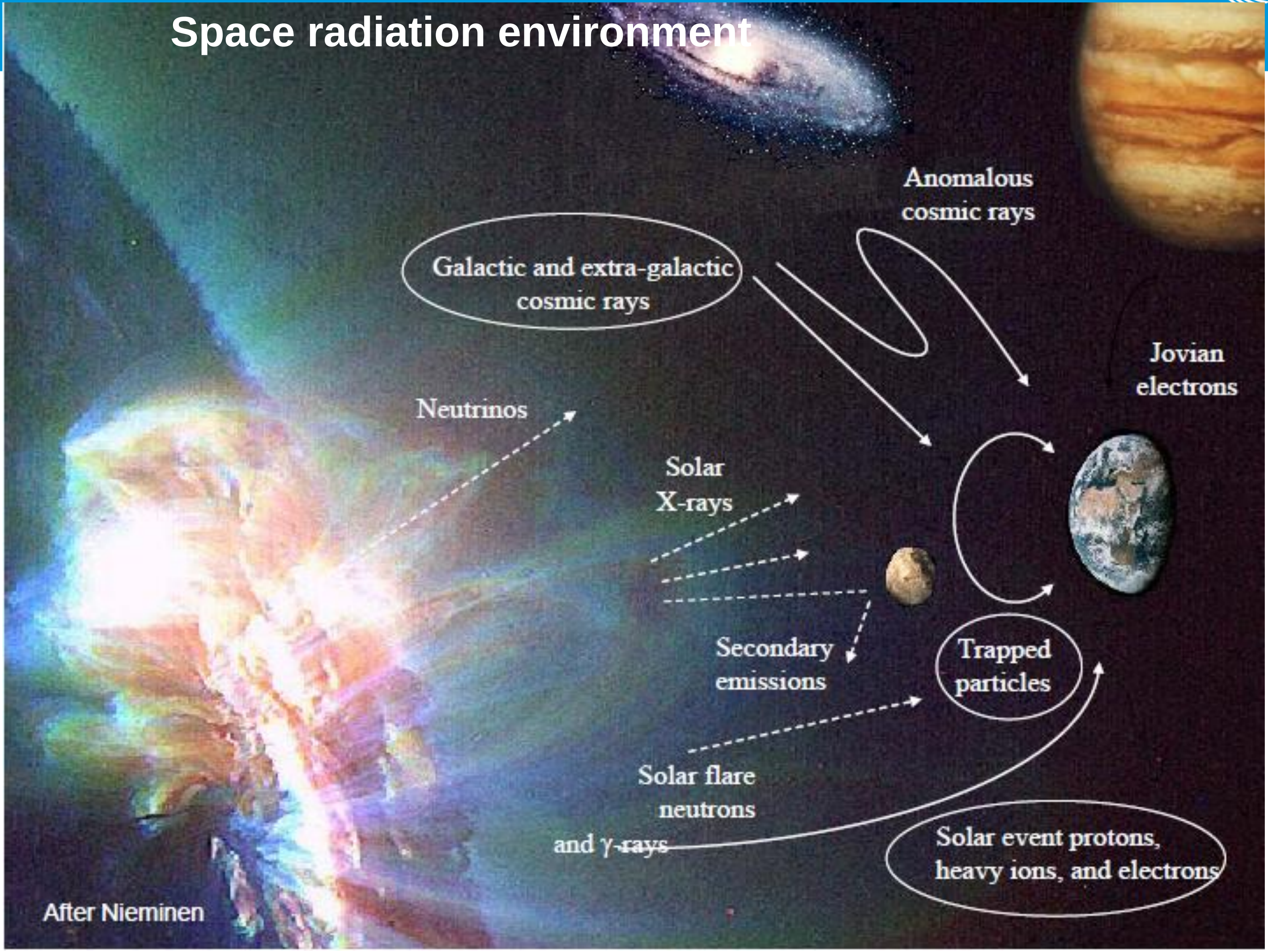
Credits: INTEL

ASICs and FPGAs in space: why could they fail?



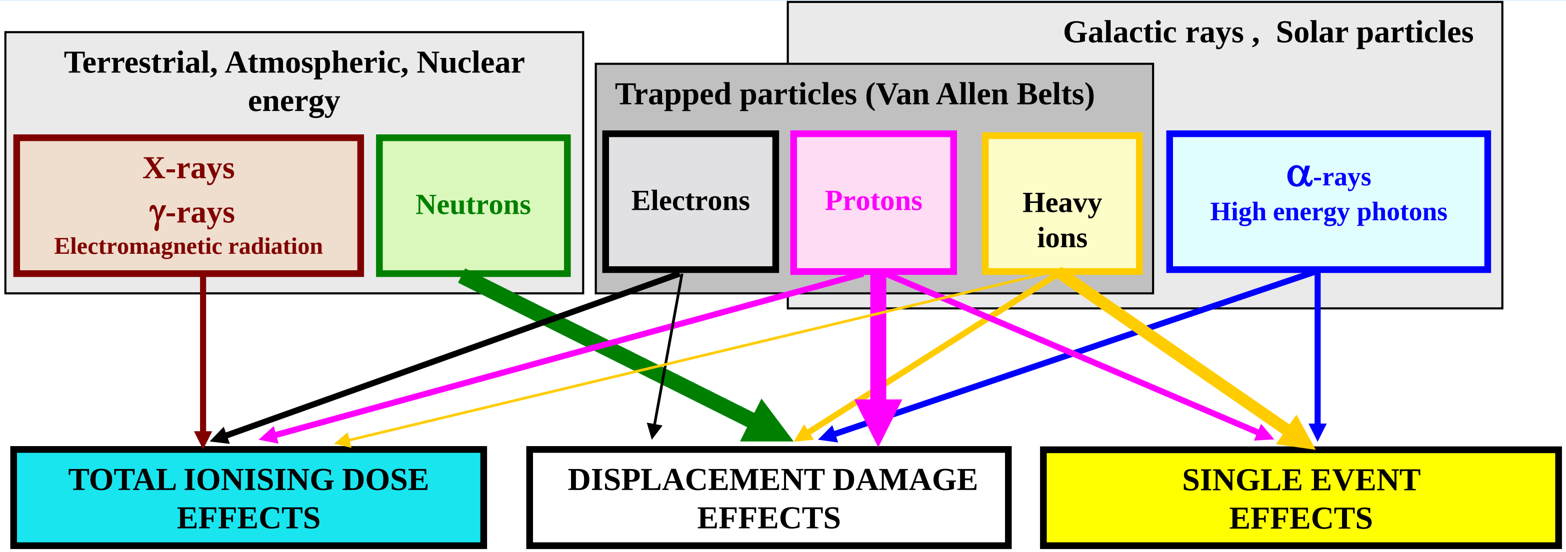
1. **Designer mistake**
   - Some nominal or corner cases never simulated, etc.
2. **Manufacturing problem or error**
   - Silicon wafer defects
   - badly calibrated machine
   - operator error
   - poor, insufficient error screening, etc.
3. **System environment**
   - out-of-spec use (wrong bias, pin load, clock…)
   - signal integrity problems at PCB, etc.
4. **Aging effects – technology wear-out**
   - Electro migration
   - Channel hot carriers
   - Negative bias temperature instability (NBTI), etc, etc.
5. **Space environment effects**
   - Vibration, mechanical shock (bonding, solder points failures)
   - Extreme temperatures
   - Contamination effects
   - Radiation effects

Space radiation environment



After Nieminen

Radiation Effects in semiconductor devices



♦ effects in semiconductor elements

→effects in basic analogue and digital cells

♦Creation of electron-hole pairs
♦Charge build-up, excitation, transport

→Threshold voltage negative shift in n-channel
→Threshold voltage shift in parasitic transistors in bulk or thick epi layers
→Reduction of mobility in channel conductance and transconductance
→Increase of standby / off-state / leakage current
→changes in circuit parameters: operating point, gain, impedance, drive

♦Atomic dislocation, nuclear displacement in lattice
♦Reduction in mobility
♦Reduction in carrier concentration
♦Increase in dangling bonds / free radicals
♦Increased defect concentration
♦"rapid annealing" of minority carrier lifetime
♦More defects, accelerated aging (shorter life time)

→changes in circuit parameters: operating point, gain, impedance, drive

♦Local Ionisation (volume effects)
→**Single Event Latch-Up** **(SEL)** activation of parasitic npnp/pnpn structures causing anomalous switching behaviour of main transistor and large draw currents. Possible permanent failure.
→**Single Event Upset** **(SEU)** temporary "bit-flip" in memory element caused by internal charge deposition
→**Single Event Transient** **(SET)** transient current or voltage spike. If propagated and latched by memory element, may result in "bit-flip"
→**Single Hard Errors** **(SHE)** such as gate/dielectric rupture, burn-out, in high V junctions transversed by heavy ions

Radiation propagating EFFECTS

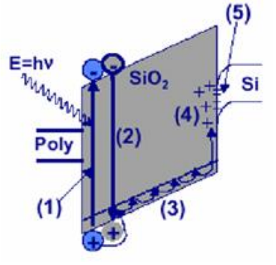
effects in semiconductor elements

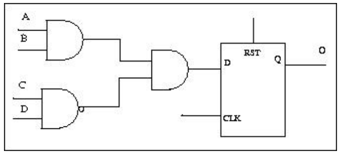
effects in basic analogue and digital cells

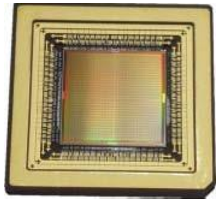
failing devices, components

failing units, sub-systems

failing onboard experiments, spacecrafts!!

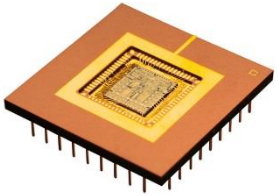






Why radiation effects in ASICs and FPGAs are a concern?

unprotected



+

Extreme T environment,
Si defects,
Aging effects

=

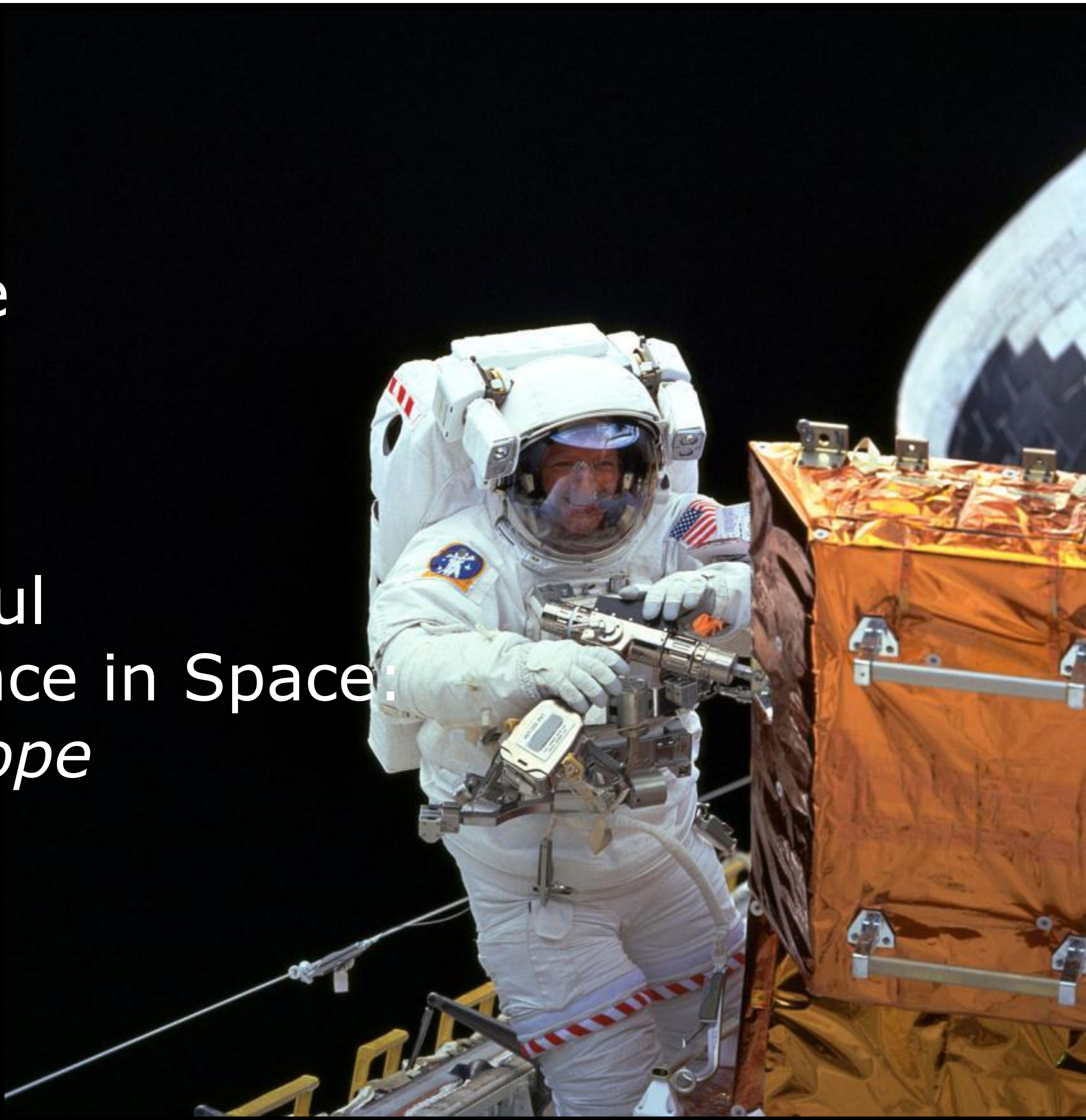
BIG TROUBLE

- temporary or permanent IC malfunctions

- risk of mission failures or loss

- on-board IC replacement or repair not an option

Repairs in Space



- Normally not possible
- Extremely costly

- Example for successful repair and maintenance in Space: *Hubble Space Telescope*

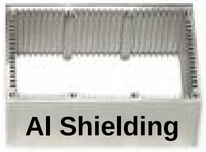
Rad Effects in ASICs and FPGAs: Countermeasures

How to classify them?

WHO implements them?

- system HW and SW designer
- IC designer (IC Design Kit user)
- IC design (CAD) tools developer
- IC library / Design Kit / layout designer
- Foundry process & manufacturing engineer

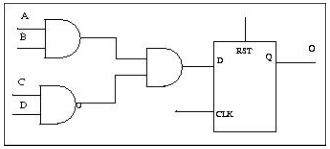
Power cycling

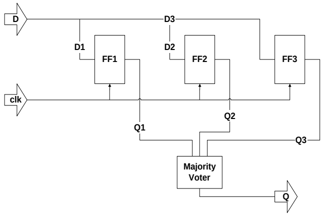

Al Shielding

scrubbing, TMR, current limiters

At which **LEVEL** are they applied?

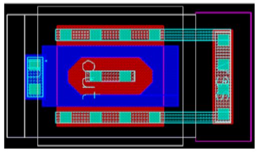
- system (PCB, software, case)
- IC architecture (netlist)
- logic cell, layout level (libraries, reset/clock lines)
- foundry process (wafer substrates, conductive, dielectric and isolating materials and sizes)

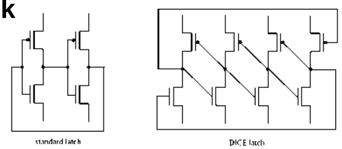




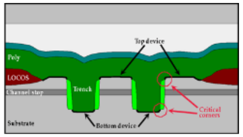
TMR, EDAC, parity, time redundancy

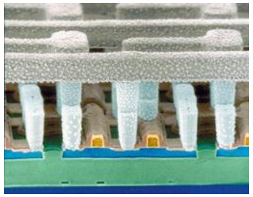
Enclosed transistors , hard FF, hard clock trees





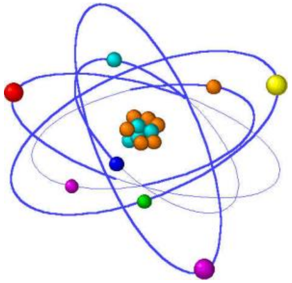
SOI, epi, thin OX, wells, STI, guardbands





Rad Effects in ASICs & FPGAs: Countermeasures

What are the **COSTS / DRAWBACKS** of rad effects protections?



-More Silicon area, less integration

-Lower speed

-Higher power consumption

-Higher design complexity, longer development times

-Export constraints dependencies

-Higher technology prices (“special technology” + “low volume” = expensive components, additional tests and tools) !!

Rad protection can sometimes have a high price, but the cost of loosing on-board experiments or the entire satellite is much higher !!

ECSS-Q-HB-60-02 is publically available!

ECSS-Q-HB-60-02

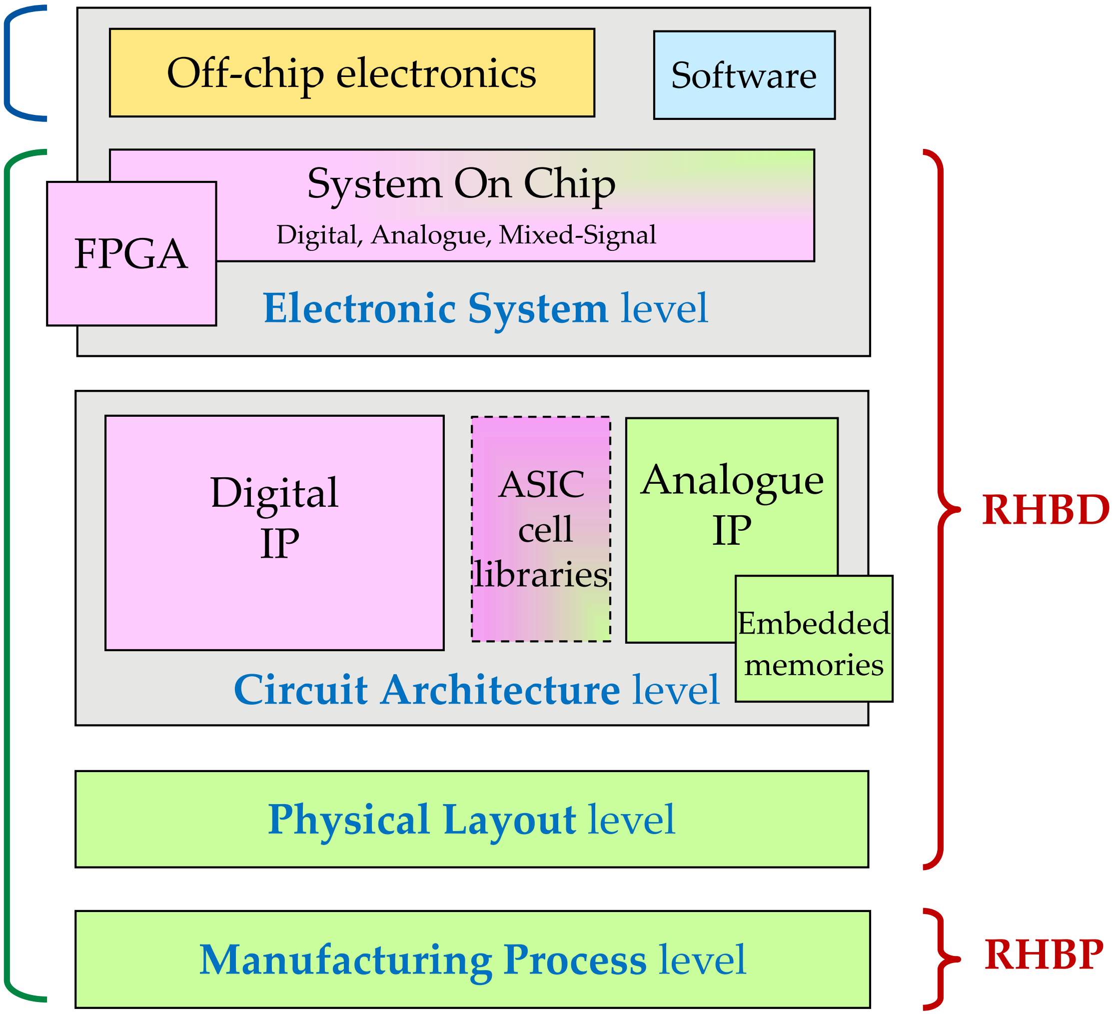
Techniques for radiation effects mitigation in ASICs and FPGAs handbook

was published on September 1st 2016, after 6 years of work and contributions from over 30 experts worldwide

==> go here: http://www.ecss.nl/

to find and download Handbook!

classification of mitigation techniques, abstraction levels



Outside
integrated circuit

Inside
integrated circuit

Techniques for radiation effects mitigation in ASICs and FPGAs handbook

ECSS-Q-HB-60-02A
1 September 2016

EUROPEAN COOPERATION
ECSS
FOR SPACE STANDARDIZATION

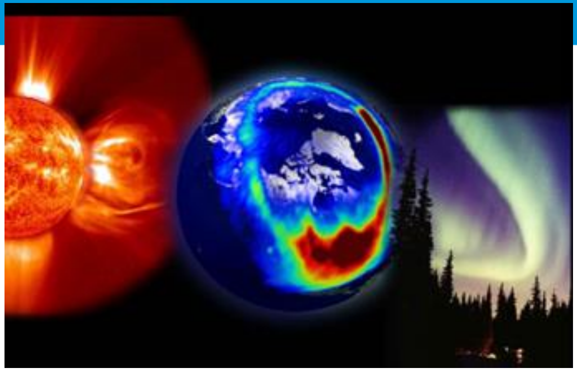
Space product assurance

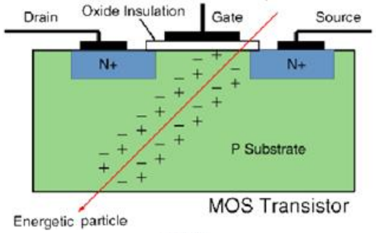
Techniques for radiation effects mitigation in ASICs and FPGAs handbook

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

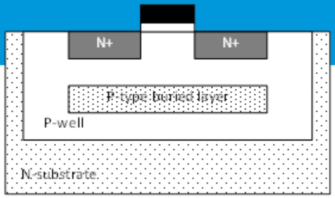
ECSS-Q-HB-60-02
published
September 1st 2016

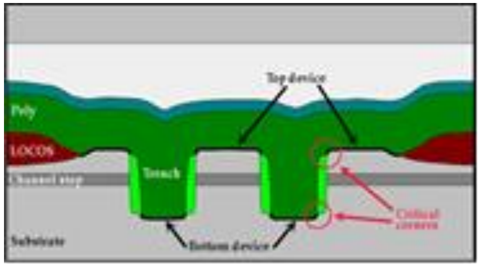
ECSS-Q-HB-60-02: the first chapters

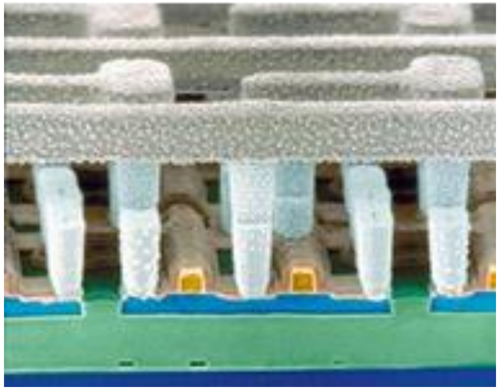




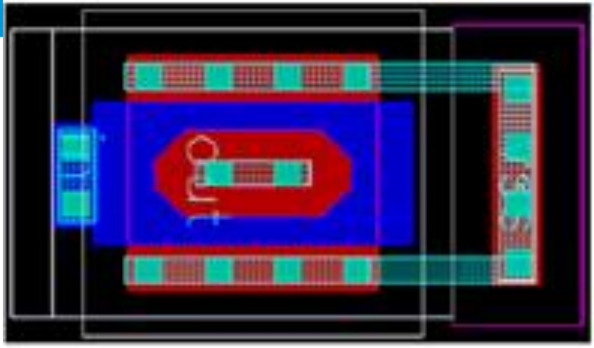
6 Technology selection and process level mitigation

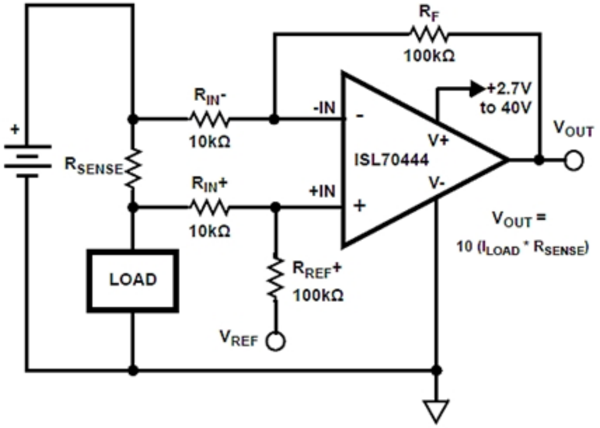


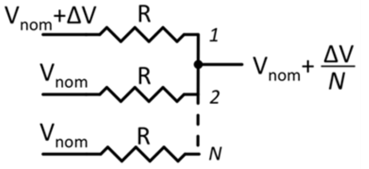




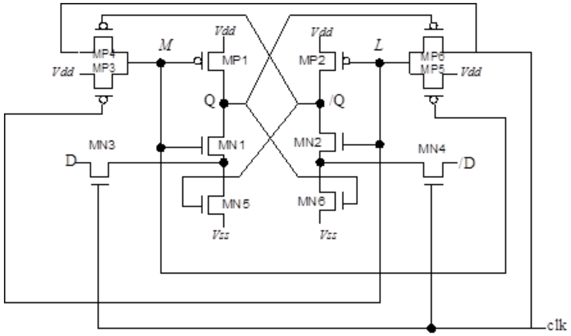
7 Layout, 8 Analogue circuits

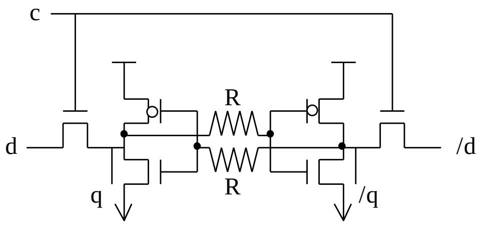




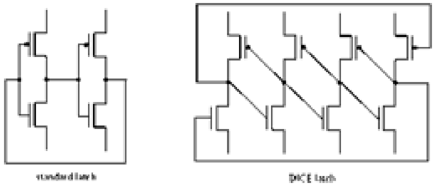


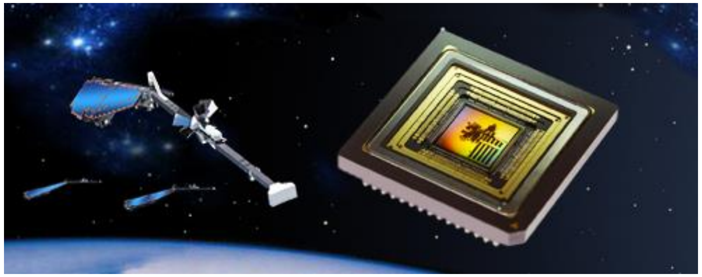
9 Embedded memories



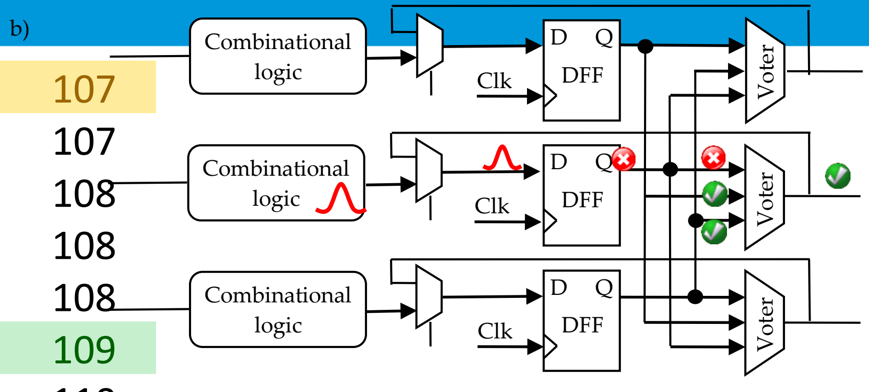


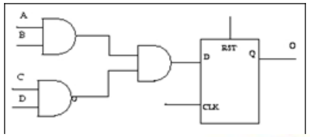
10 Radiation-hardened ASIC libraries

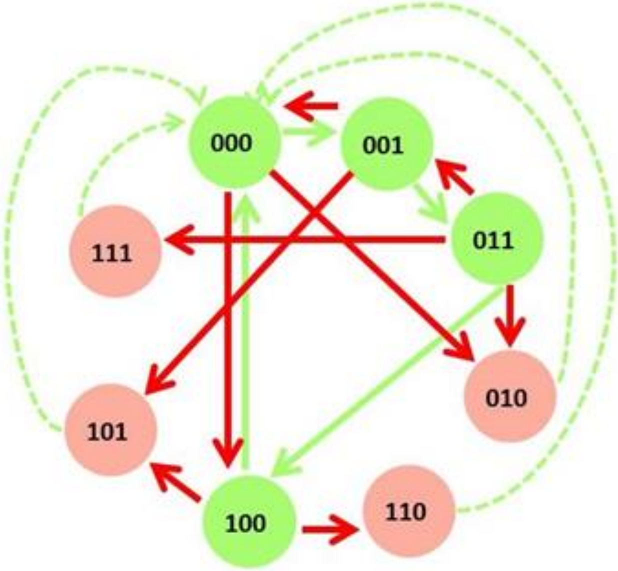




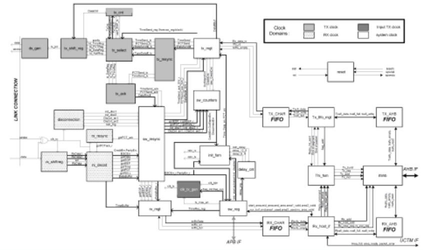
11 Digital Circuits

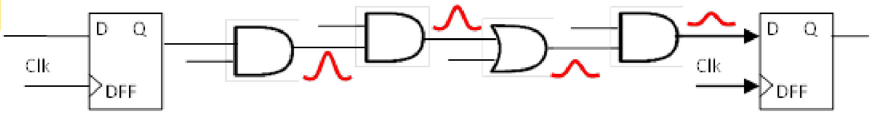


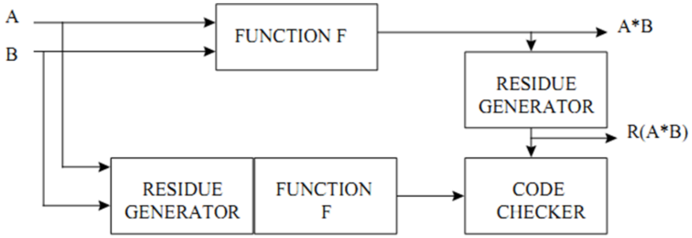




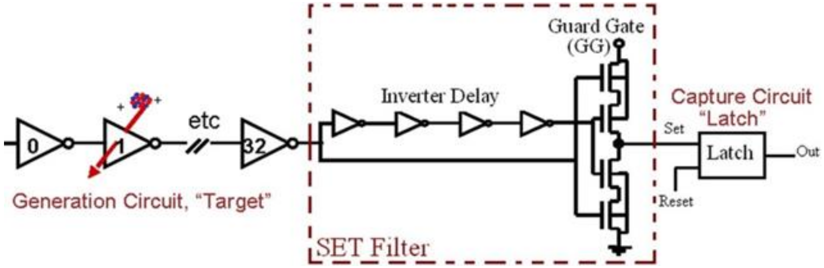
12 System on a Chip



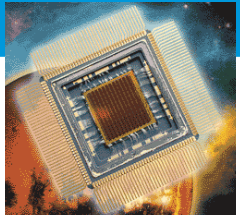




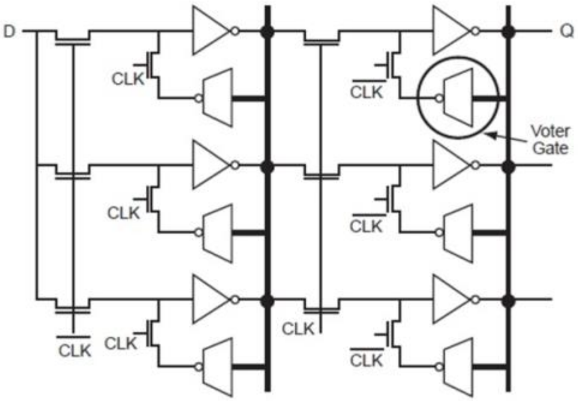
7 bits of data	Number of "1"	8-bits including parity bit	
		even	odd
000 0000	0	0000 0000	1000 0000
101 0001	3	1101 0001	0101 0001
110 1001	4	0110 1001	1110 1001
111 1111	7	1111 1111	0111 1111

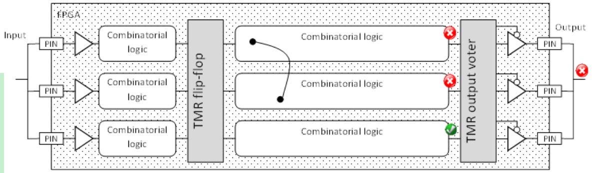


13 Field Programmable Gate Arrays



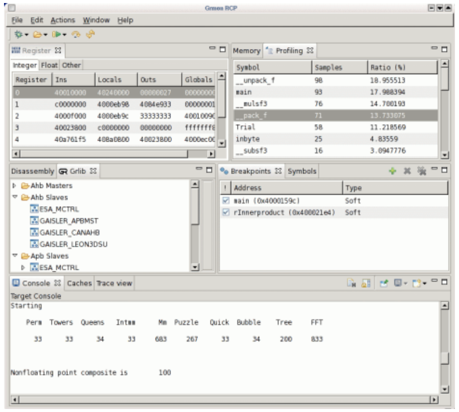
of the Virtex-5QV FPGA has been qualified for high-radiation, deep-space applications.





European Space Agency

14 Software-implemented hardware fault tolerance



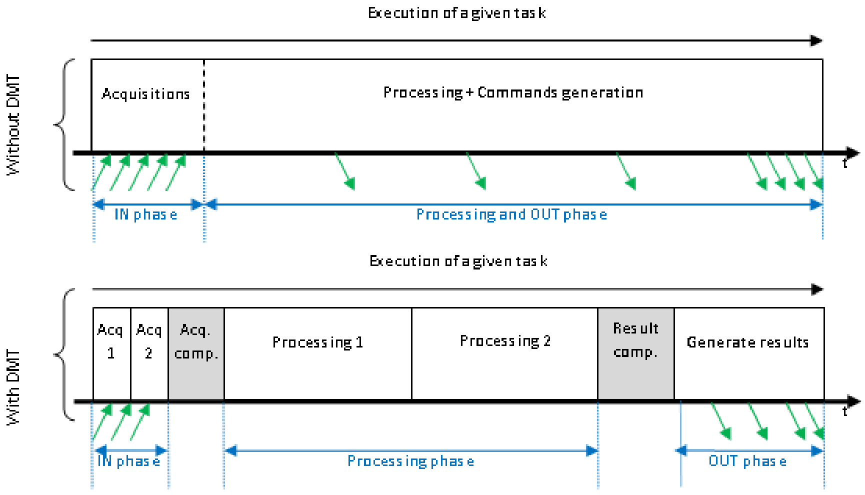
Register	Ins	Locals	Outs	Globals
0	40010000	40240000	00000027	0000000
1	c0000000	4000eb98	4084e933	00000001
2	4000f000	4000eb9c	33333333	4001009
3	40023800	c0000000	00000000	fffffff
4	40a761f5	408a0800	40023800	4000ec0

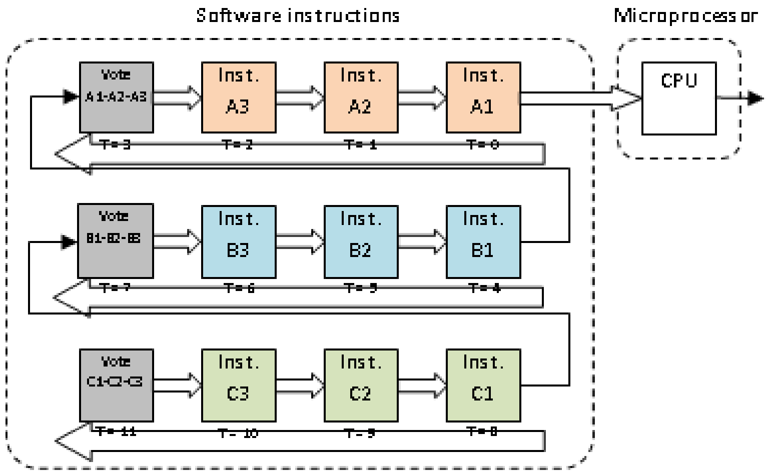
Symbol	Samples	Ratio (%)
__unpack_f	98	18.955513
main	93	17.988394
__mulsf3	76	14.700193
__pack_f	71	13.733075
Trial	58	11.218569
inbyte	25	4.83559
__subsf3	16	3.0947776

- ▷ Ahb Masters
- ▽ Ahb Slaves
  - ESA_MCTRL
  - GAISLER_APBMST
  - GAISLER_CANAHB
  - GAISLER_LEON3DSU
- ▽ Apb Slaves
  - ▷ ESA_MCTRL

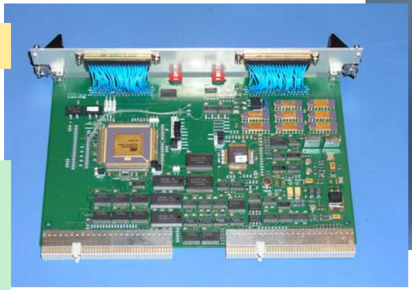
!	Address	Type
☑	main (0x4000159c)	Soft
☑	rInnerproduct (0x400021e4)	Soft

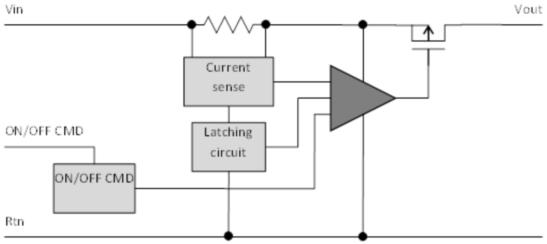
```
Starting

   Perm  Towers  Queens   Intmm     Mm  Puzzle   Quick  Bubble    Tree     FFT

     33      33      34      33    683     267      33      34     200     833



Nonfloating point composite is        100
```



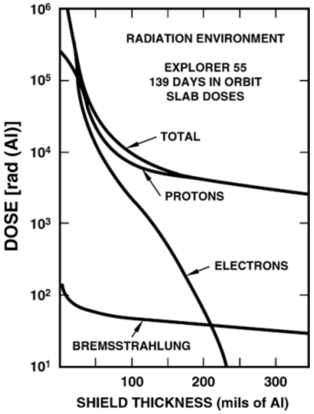


15 System architecture (off-chip)

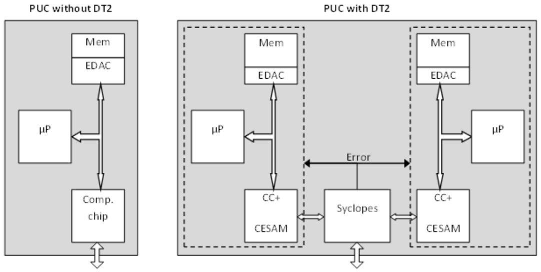




Power cycling

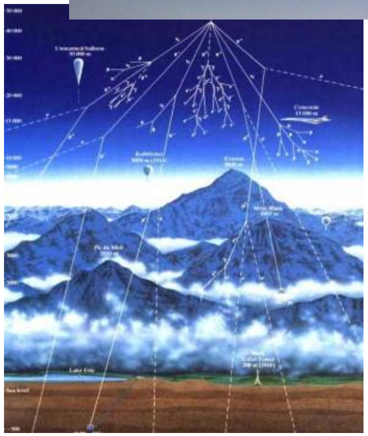


Al Shielding

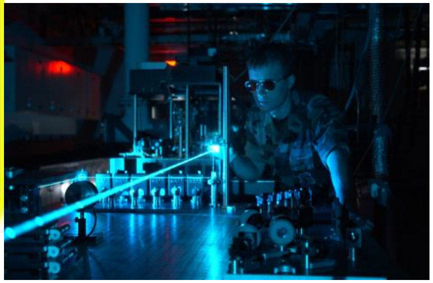


16 Validation methods (1/2)

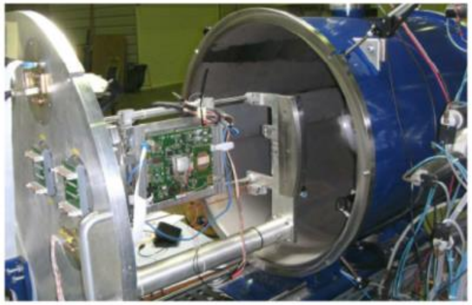
Fault Injection Testing



16 Validation methods (2/2)



- ***Radiation Facilities in use by ESA*** https://escies.org/ReadArticle?docId=230
  - Co-60 at ESA/ESTEC, Netherlands (total dose)
  - Californium-252 at ESA/ESTEC, Netherlands
  - Paul Scherrer Institut (PSI), Switzerland: proton irradiation
  - Louvain la Neuve (UCL), Belgium: heavy ions and protons
  - Jyväskylä University, Finland: heavy ions and protons



ECSS-Q-HB-60-02 is publically available!

78 mitigation techniques

classified in 10 groups

15 validation techniques

ECSS-Q-HB-60-02

Techniques for radiation effects mitigation in ASICs and FPGAs handbook

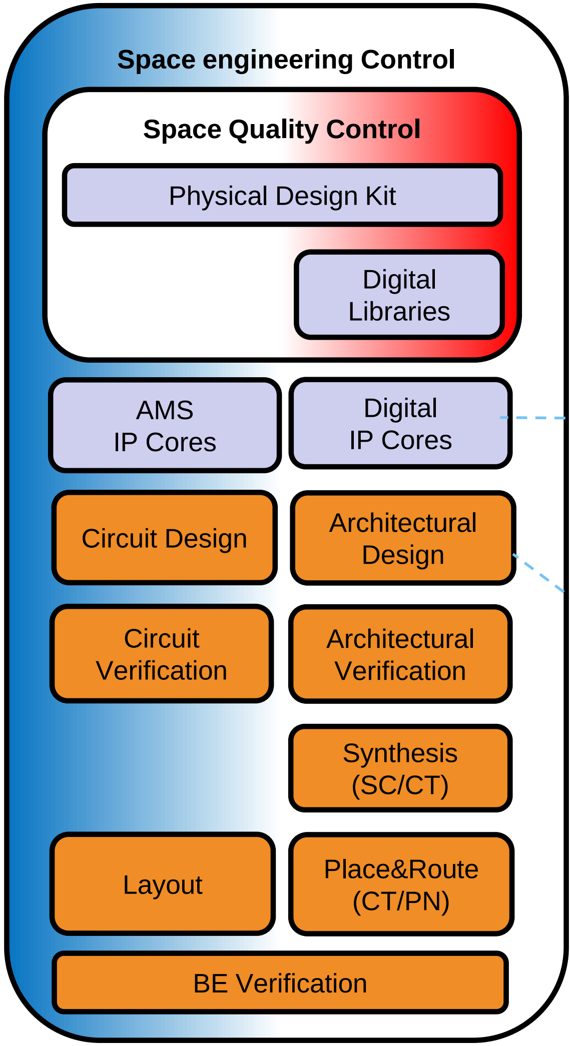
This new ECSS handbook is since September 8th 2016 available from the www.ecss.nl website, at
http://ecss.nl/forums/ecss/_templates/default.htm?target=http://ecss.nl/forums/ecss/dispatch.cgi/publications/docProfile/100219/d20160905090457/No/t100219.htm

Two additional documents available for download at the ESA Microelectronics website :
http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/Microelectronics_Development_Methodology

1. **ECSS-Q-HB-60-02A Annex** (informative) Vendor- or institute-ready ASIC and FPGA technology solutions that include mitigation against radiation effects or that can help to introduce mitigation and/or to validate it

2. **ECSS-Q-HB-60-02A Acknowledgements**

ESA Microelectronic Section Activities



Space engineering Control

Space Quality Control

Physical Design Kit

Digital Libraries

AMS IP Cores

Digital IP Cores

Circuit Design

Architectural Design

Circuit Verification

Architectural Verification

Synthesis (SC/CT)

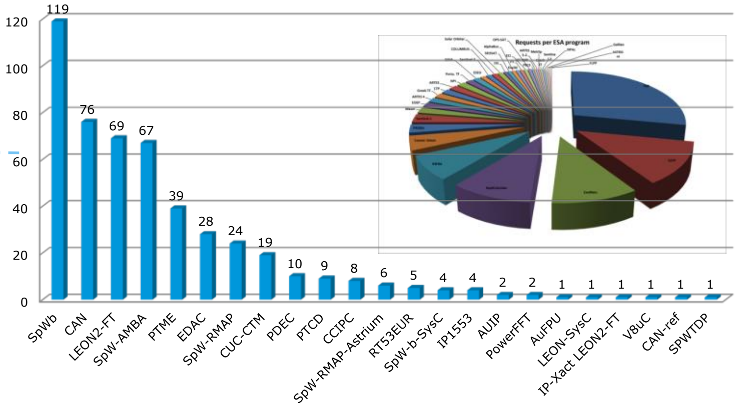
Layout

Place&Route (CT/PN)

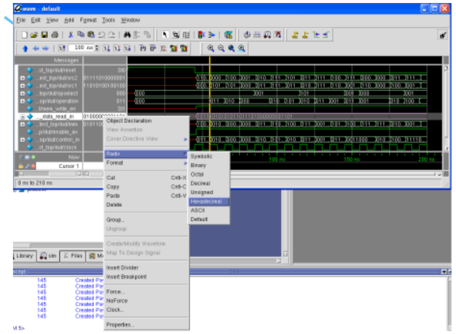
BE Verification

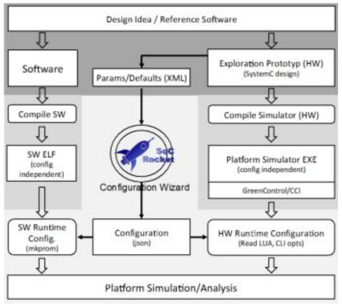
To support future microelectronics programmes, the section undertakes internal research and development

Digital IP Cores



SoC Architecture Simulation, Verification, Validation

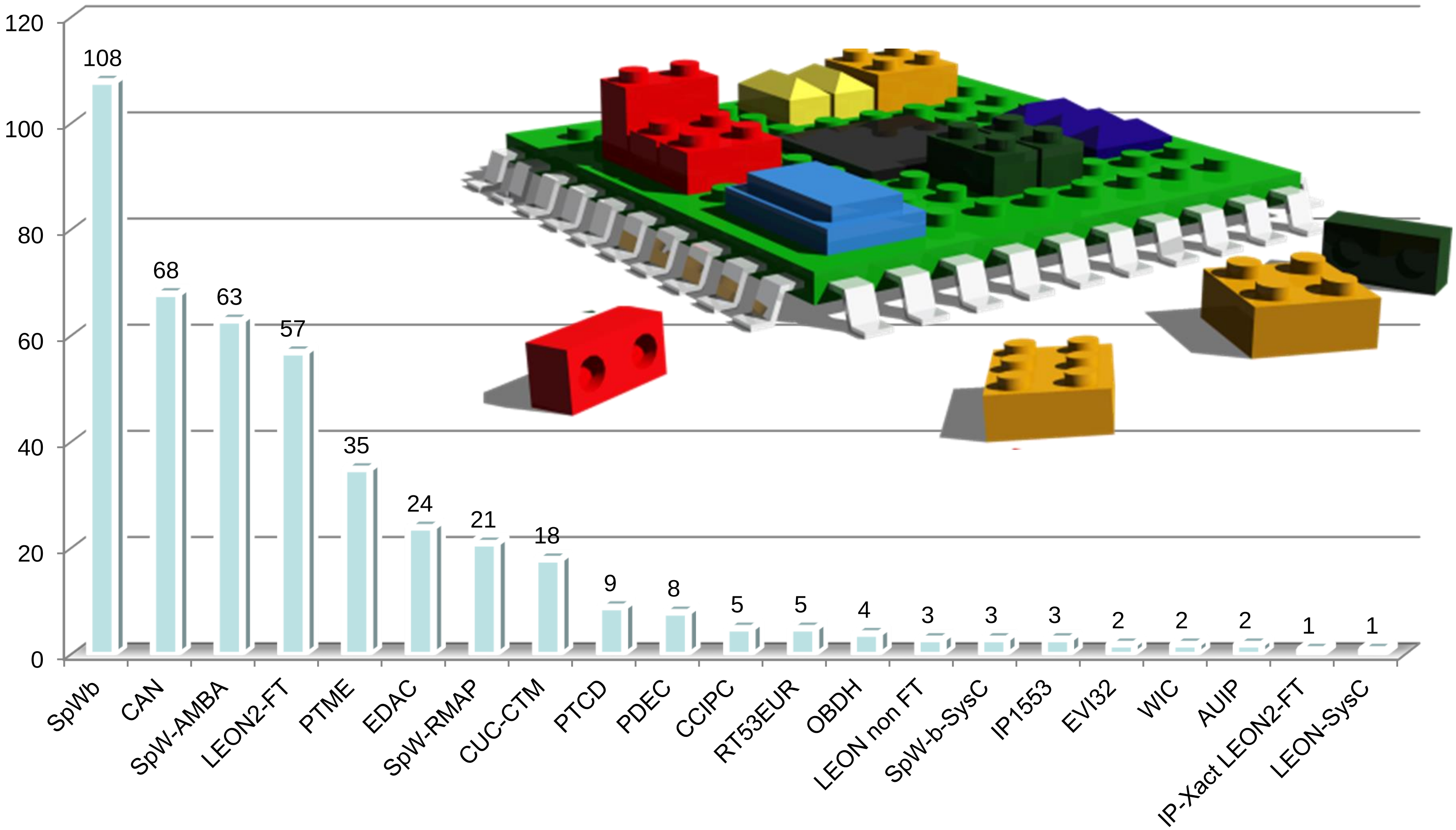




ESA IP-Core Service

Statistics

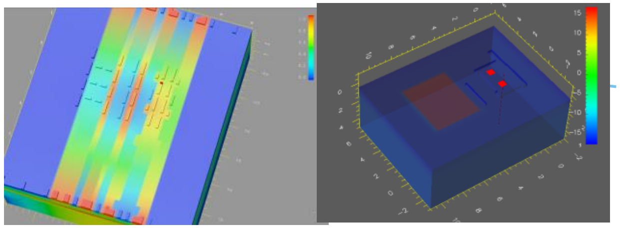
Number of Requests per IP-Core since 2002



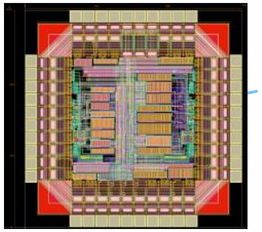
http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/About_ESA_IP_Cores

ESA Microelectronic Section Activities

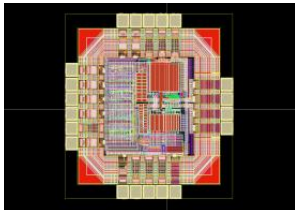
3D TCAD SET/SEU Simulations in 65nm and 180nm CMOS



SET Test Vehicle Development and Radiation Testing



AMS IP Core Development



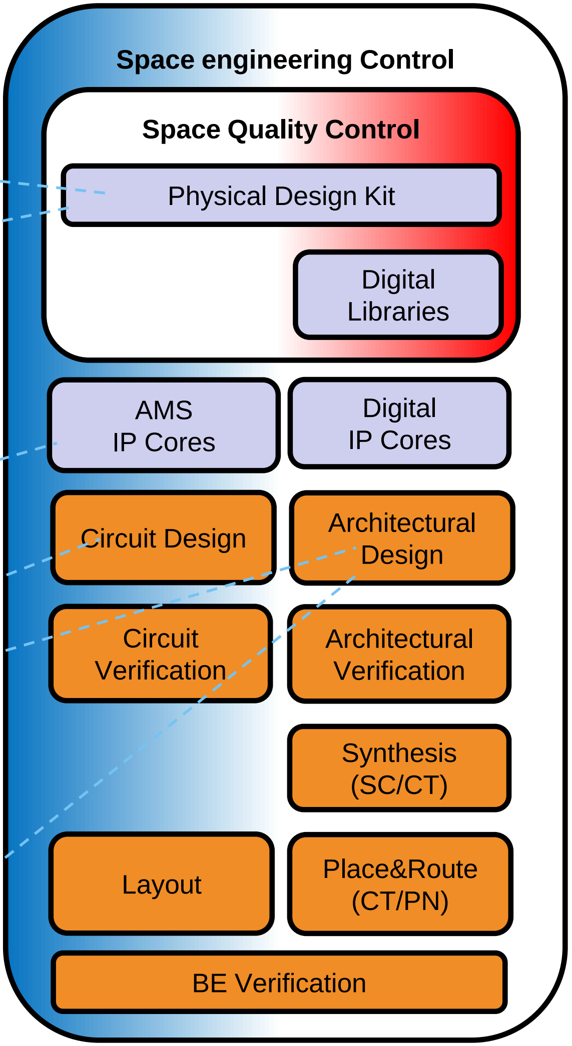
Radiation Mitigation Techniques

Space product assurance

Techniques for radiation effects mitigation in ASICs and FPGAs handbook

SEU Mitigation Validation

Ready to go



Space engineering Control

Space Quality Control

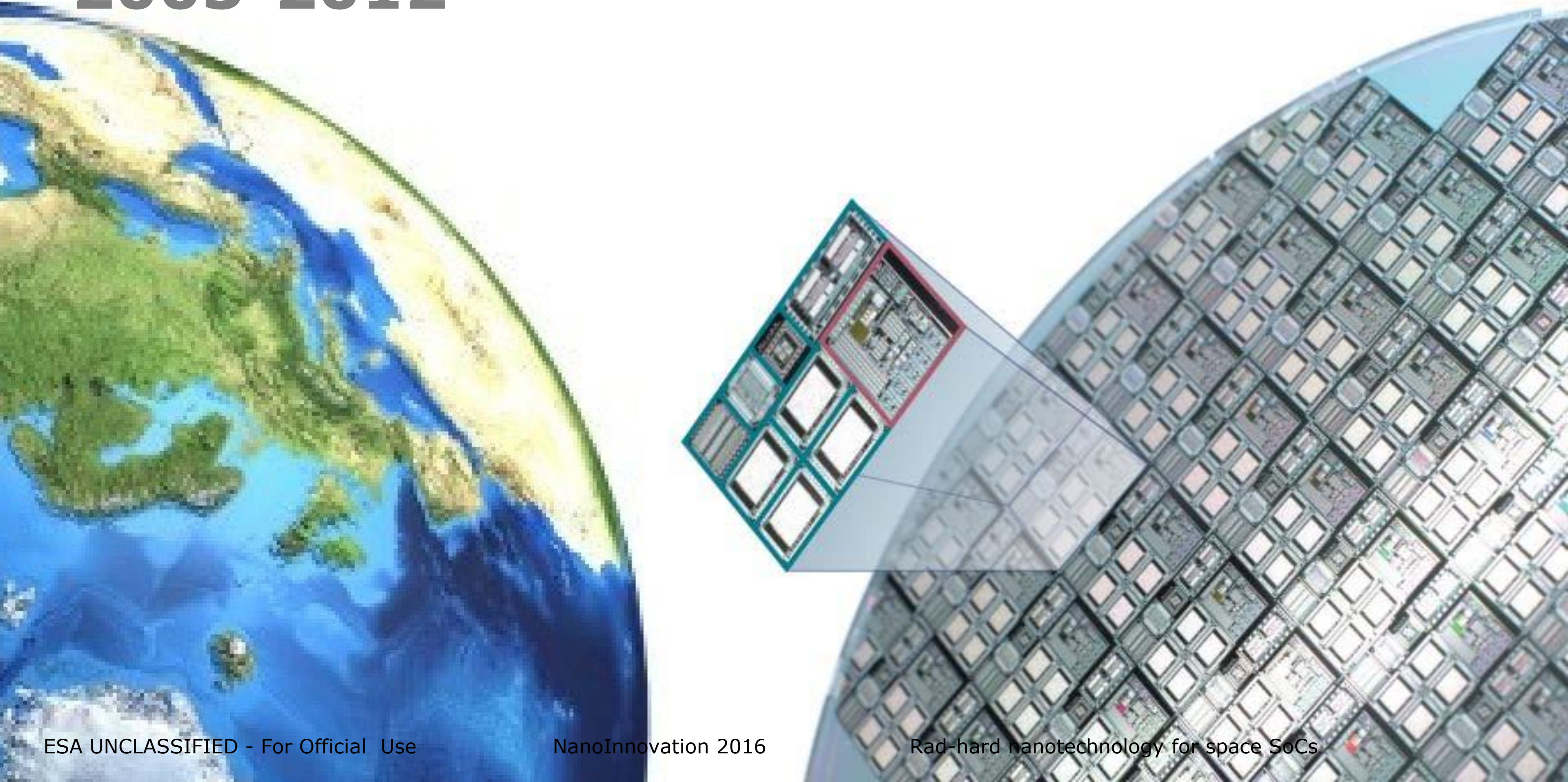
- Physical Design Kit
- Digital Libraries

- AMS IP Cores
- Digital IP Cores
- Circuit Design
- Architectural Design
- Circuit Verification
- Architectural Verification
- Synthesis (SC/CT)
- Layout
- Place&Route (CT/PN)
- BE Verification

Space Multi Project Wafer (MPW) programme

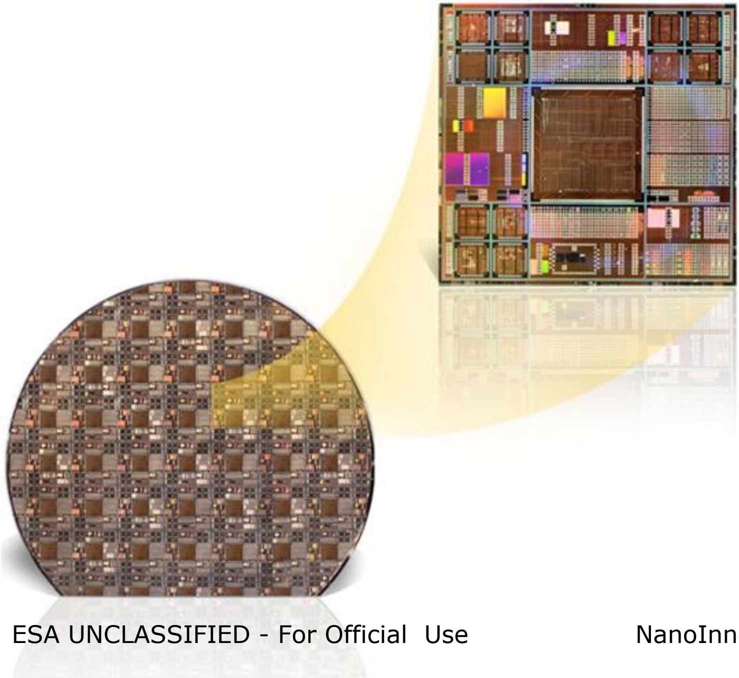
One example of ESA activity on space SoCs

2003-2012



Space Multi Project Wafer (MPW) programme

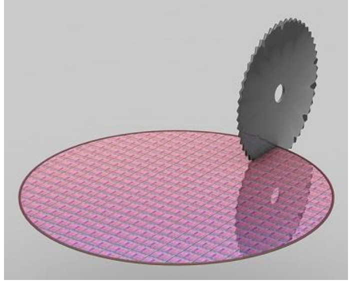
- **GOALS**

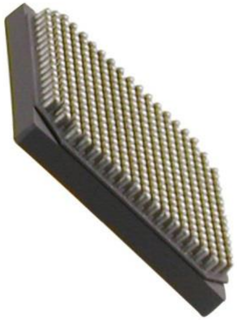


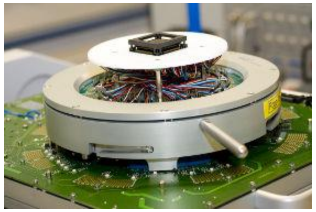
  - 2003: new space digital ASIC technology Atmel(F) **ATC18RHA** (180nm CMOS)
  - facilitate access, encourage use
  - **Lower chip prices**: grouping customers/designs to share silicon wafer manufacturing costs

Space Multi Project Wafer (MPW) programme

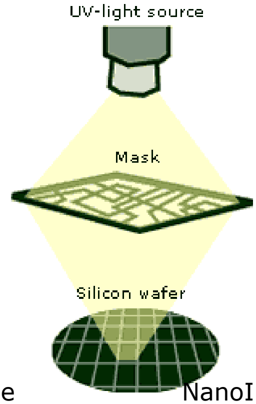
CREATING an ASIC

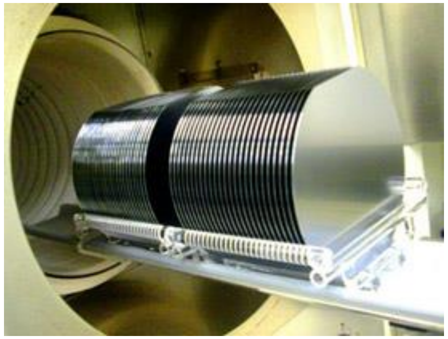






Specs -> Design -> Masks -> Wafers -> Dicing -> Packaging -> Tests

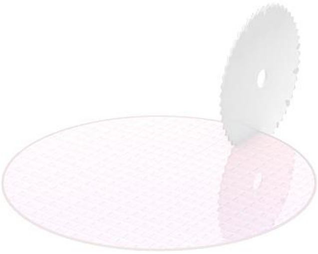




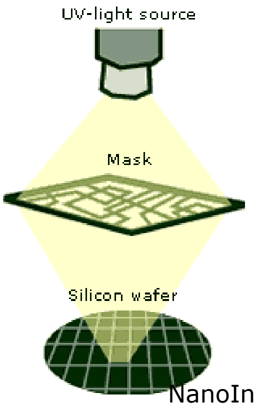
Space Multi Project Wafer (MPW) programme

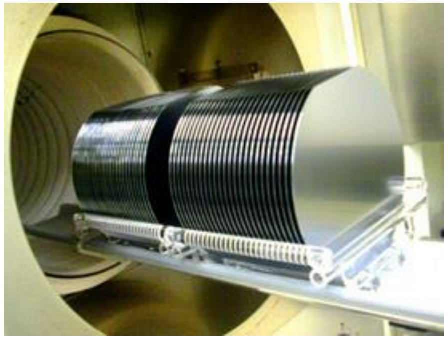
Design & manufacturing of 6 mask-sets, and 6 "lots" of 25 wafers each





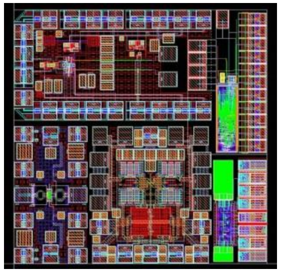
Specs -> Design -> **Masks** -> **Wafers** -> Dicing -> Packaging -> Tests



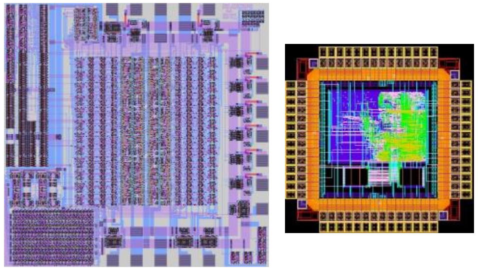


Space Multi Project Wafer (MPW) programme

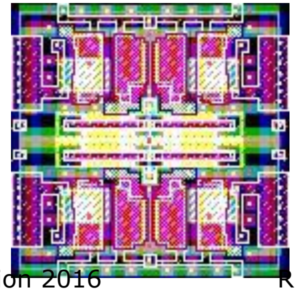
Company A → ASIC Design A



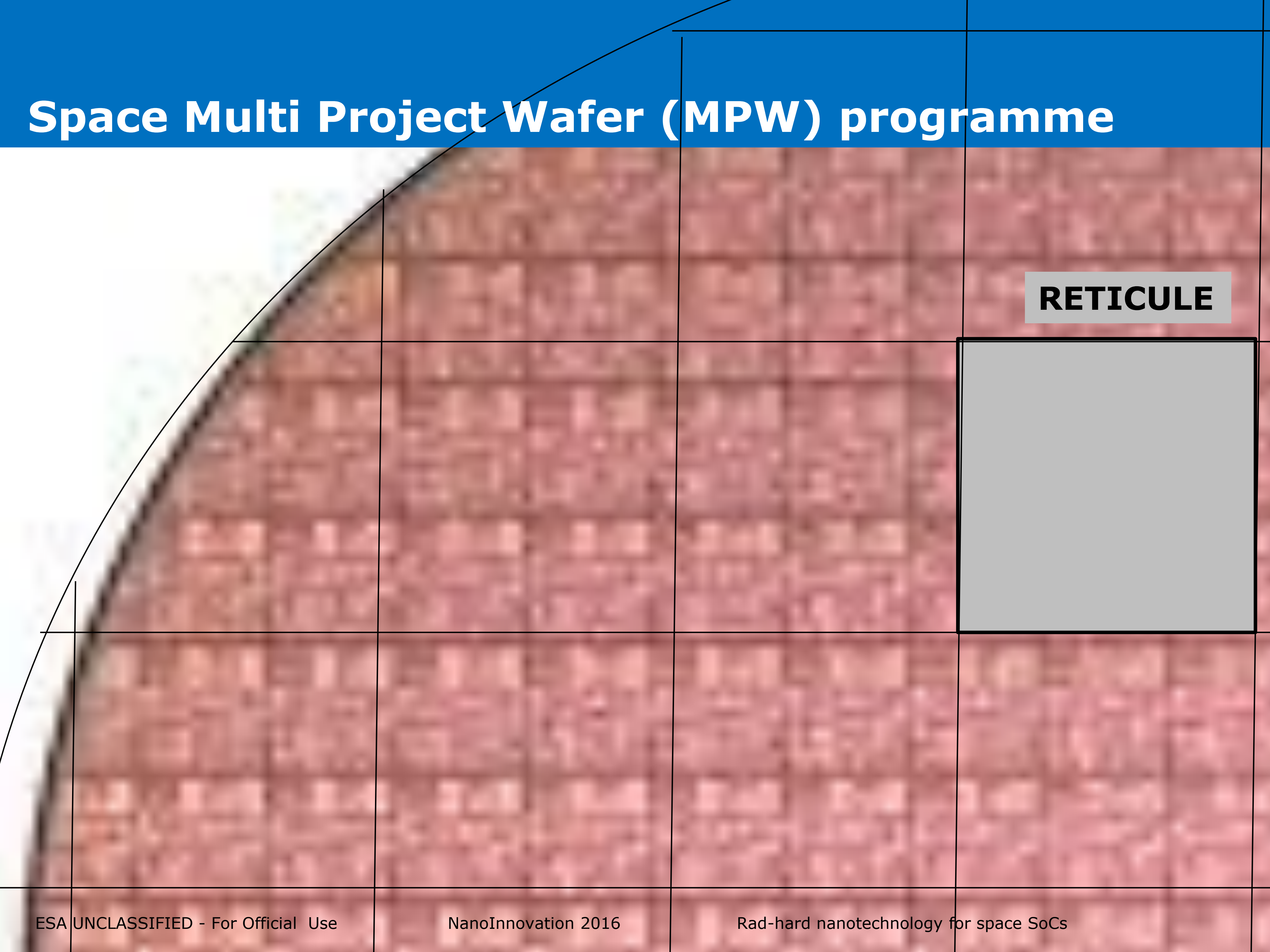
Company B → ASIC Designs B1 & B2



Company C → ASIC Design C

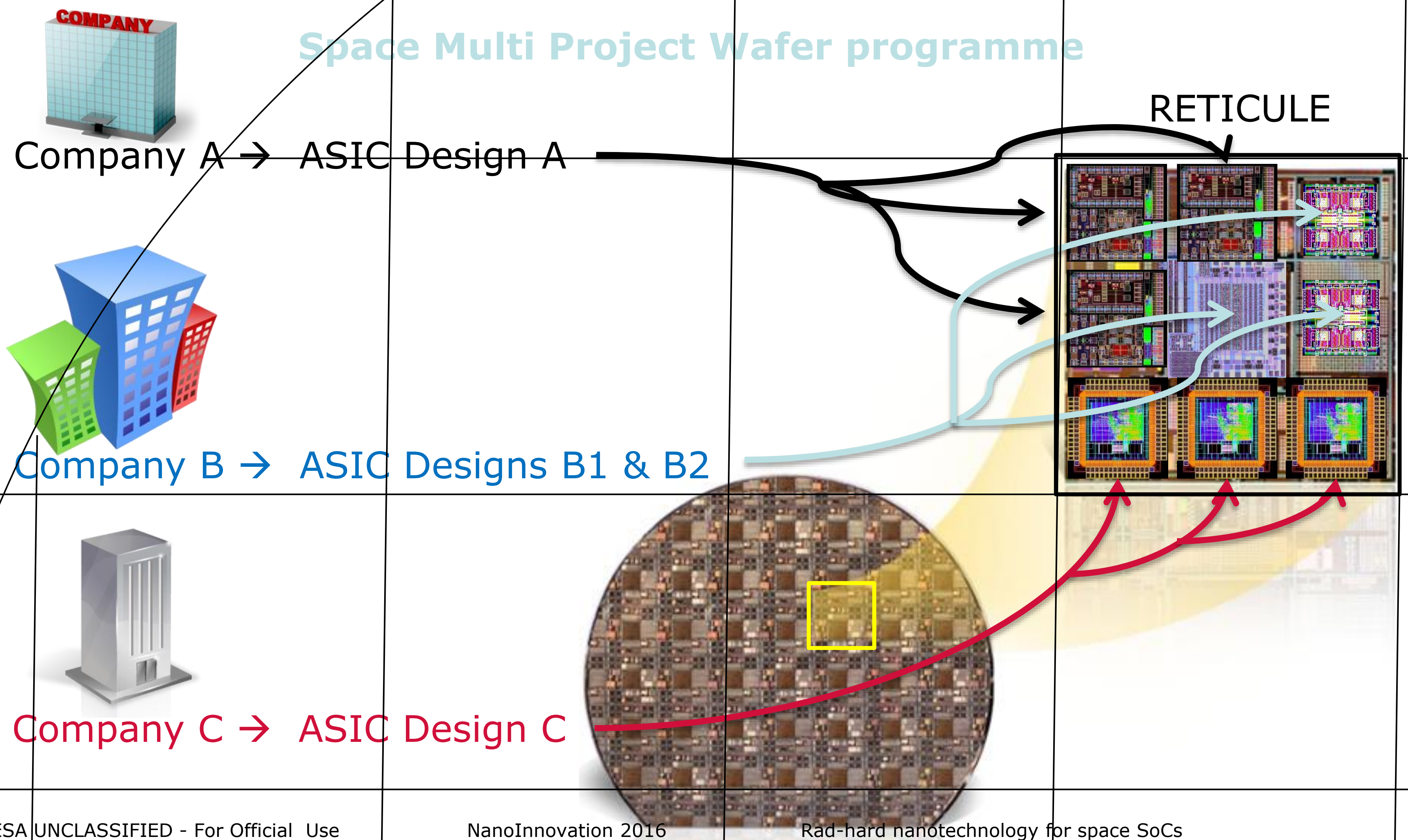


Space Multi Project Wafer (MPW) programme



Space Multi Project Wafer (MPW) programme

Space Multi Project Wafer programme



Company A → ASIC Design A

Company B → ASIC Designs B1 & B2

Company C → ASIC Design C

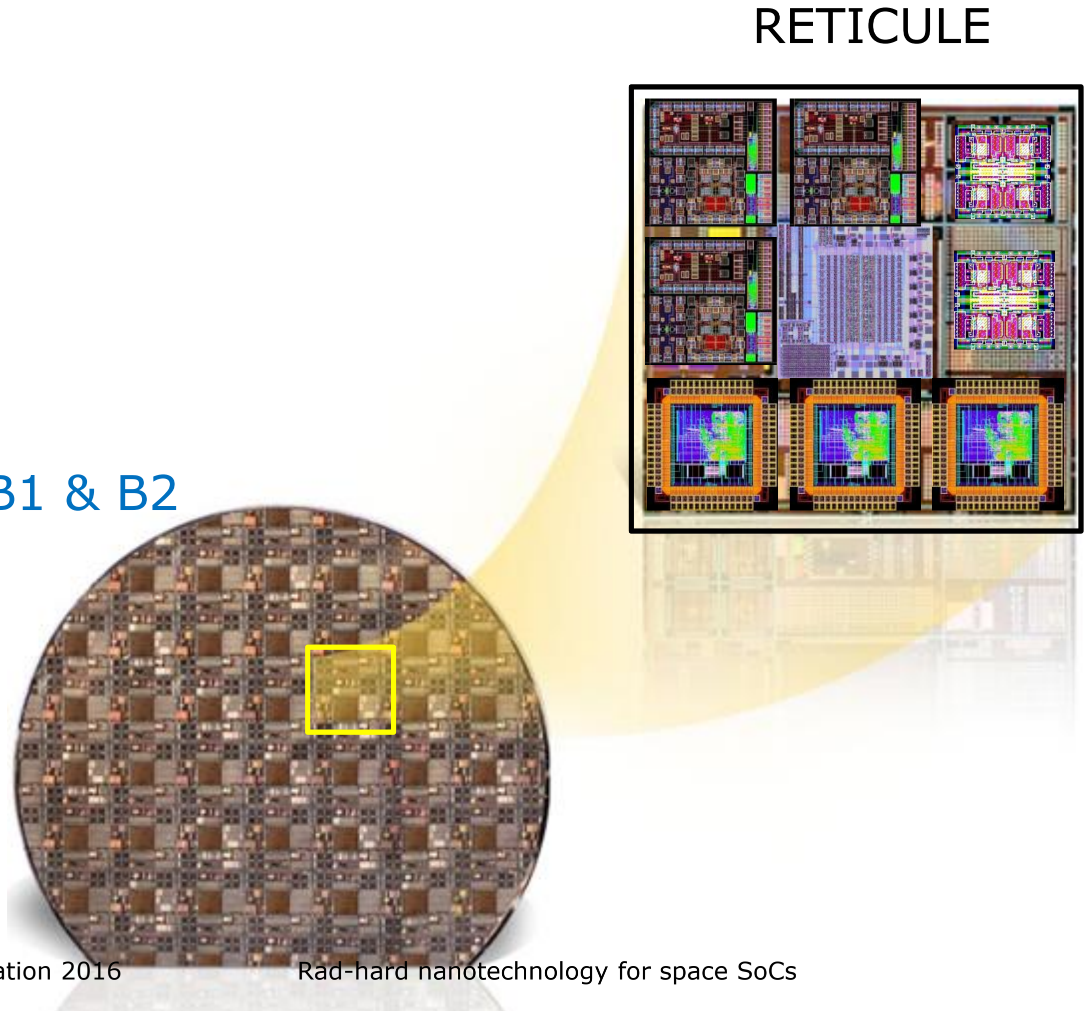
Space Multi Project Wafer (MPW) programme

Space Multi Project Wafer programme

Company A → ASIC Design A

Company B → ASIC Designs B1 & B2

Company C → ASIC Design C

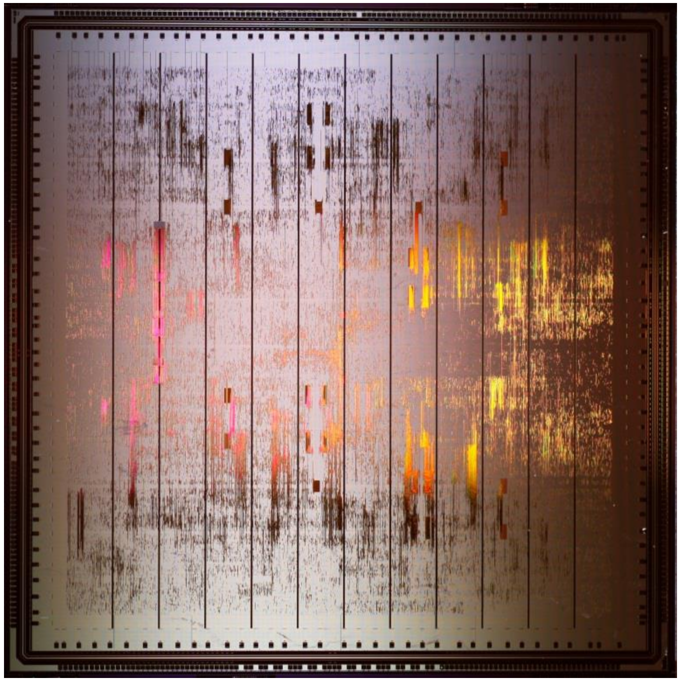


Space Multi Project Wafer (MPW) programme

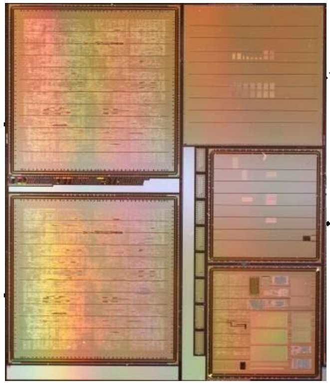
E0 run: 2004
“Validation Run”

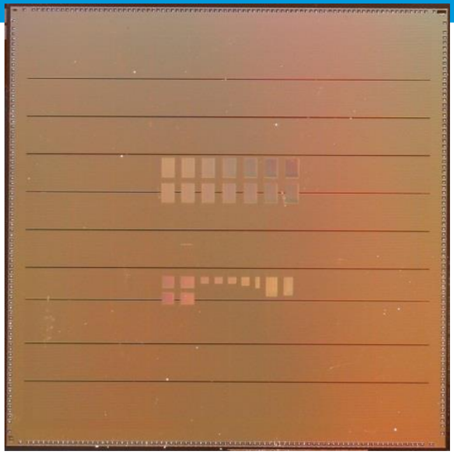
QDMX

Designed by: Alcatel SAS (F)
Function: Telecom payload mux demux



wafer “**reticule**”
(replicated 25 times
inside every wafer)



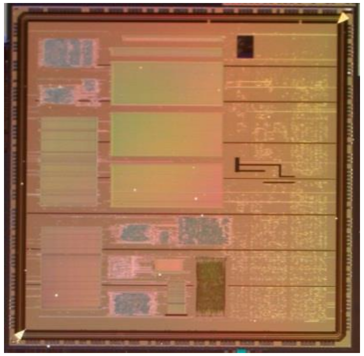


NPM-A

Designed by: Astrium (UK)
Function: Telecom payload

V34

Designed by: Atmel(F)
Function: Test Vehicle



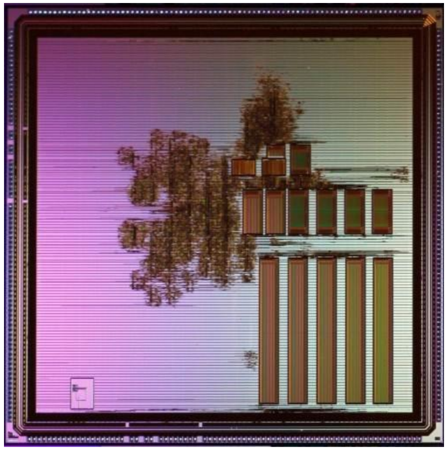
V35

Designed by: Atmel(F)
Function: Test Vehicles

E1 run: 2007

SpW-RTC (SpaceWire Remote Terminal Controller)

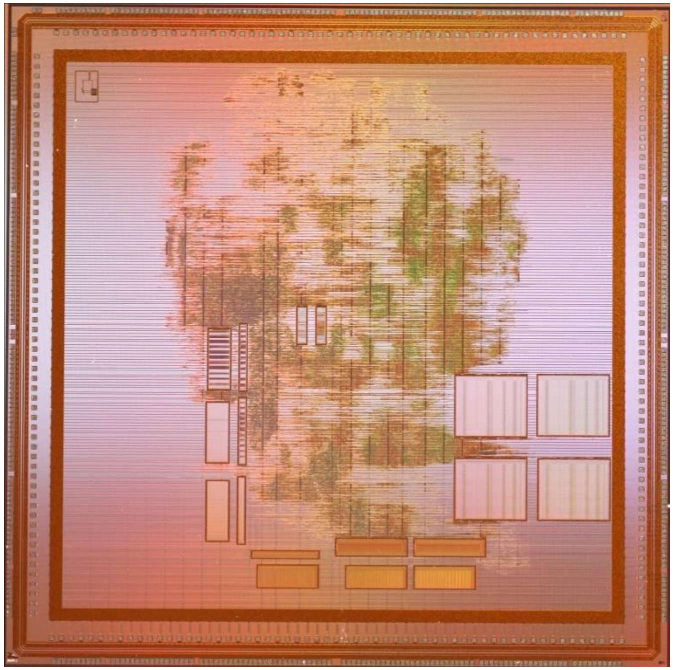
Designed by: Saab (S) + Gaisler Research (S)
Function: SpaceWire+CAN+LEON2
Flying in : **BepiColombo, Solar Orbiter**

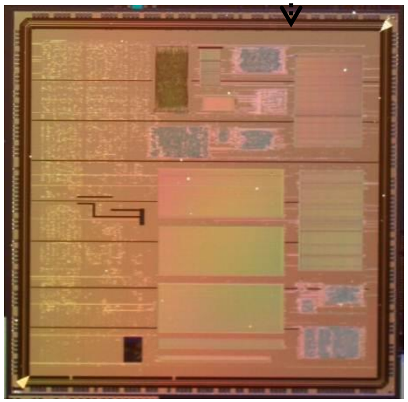


wafer “**reticule**”
(replicated 40 times
inside every wafer)

COLE

Designed by: Saab (S)
Function: LEON2 + I/O coprocessor + CAN + SpW
Flying in: **SmallGEO, MTG**

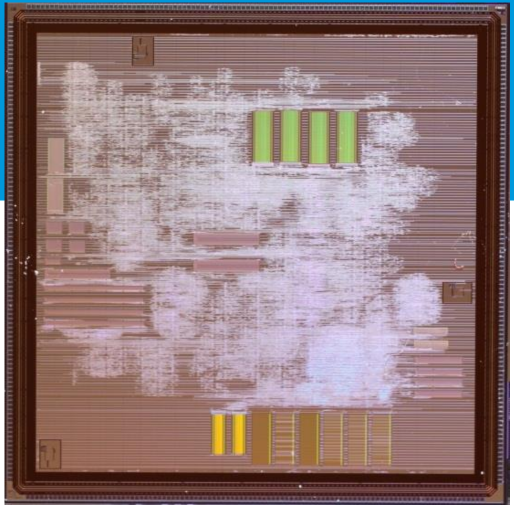




V40

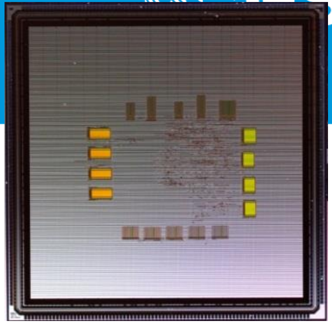
Designed by: Atmel(F)
Function: Test Vehicle

E2 run: 2008



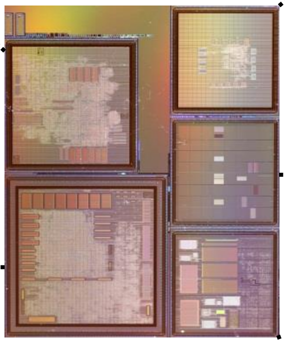
MDPA (Multi-DSP/Microprocessor Architecture)

Designed by: EADS Astrium (D)
Function: Digital Transparent Processor payload control
Flying in: **Alphasat**

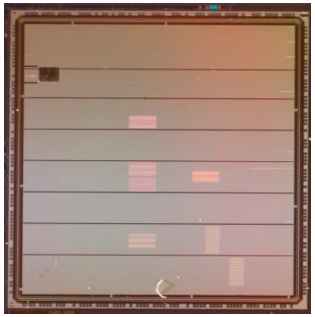


(Active Pixel Sensor Star Sensor) **APSS**

Designed by: Jena Optronik(D)
Function: Star Tracker control

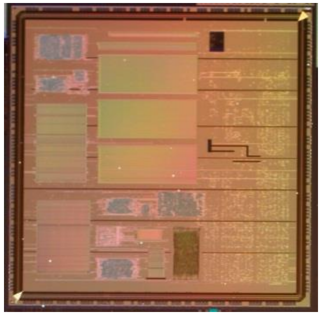


wafer "**reticule**"
(replicated 35 times
inside every wafer)



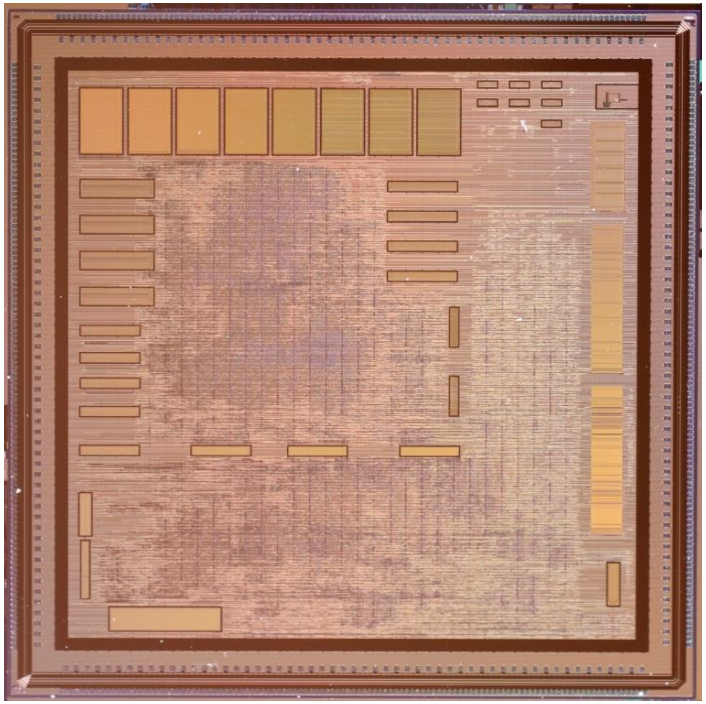
V47

Designed by: Atmel(F)
Function: Test Vehicle



V40

Designed by: Atmel(F)
Function: Test Vehicle

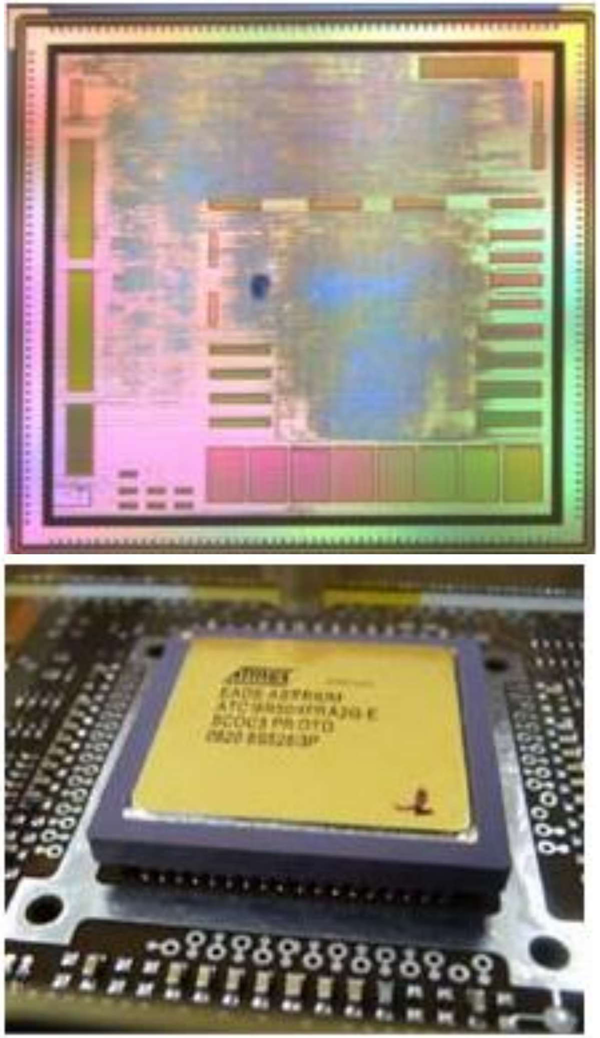


SCOC3 (Spacecraft Controller on Chip)

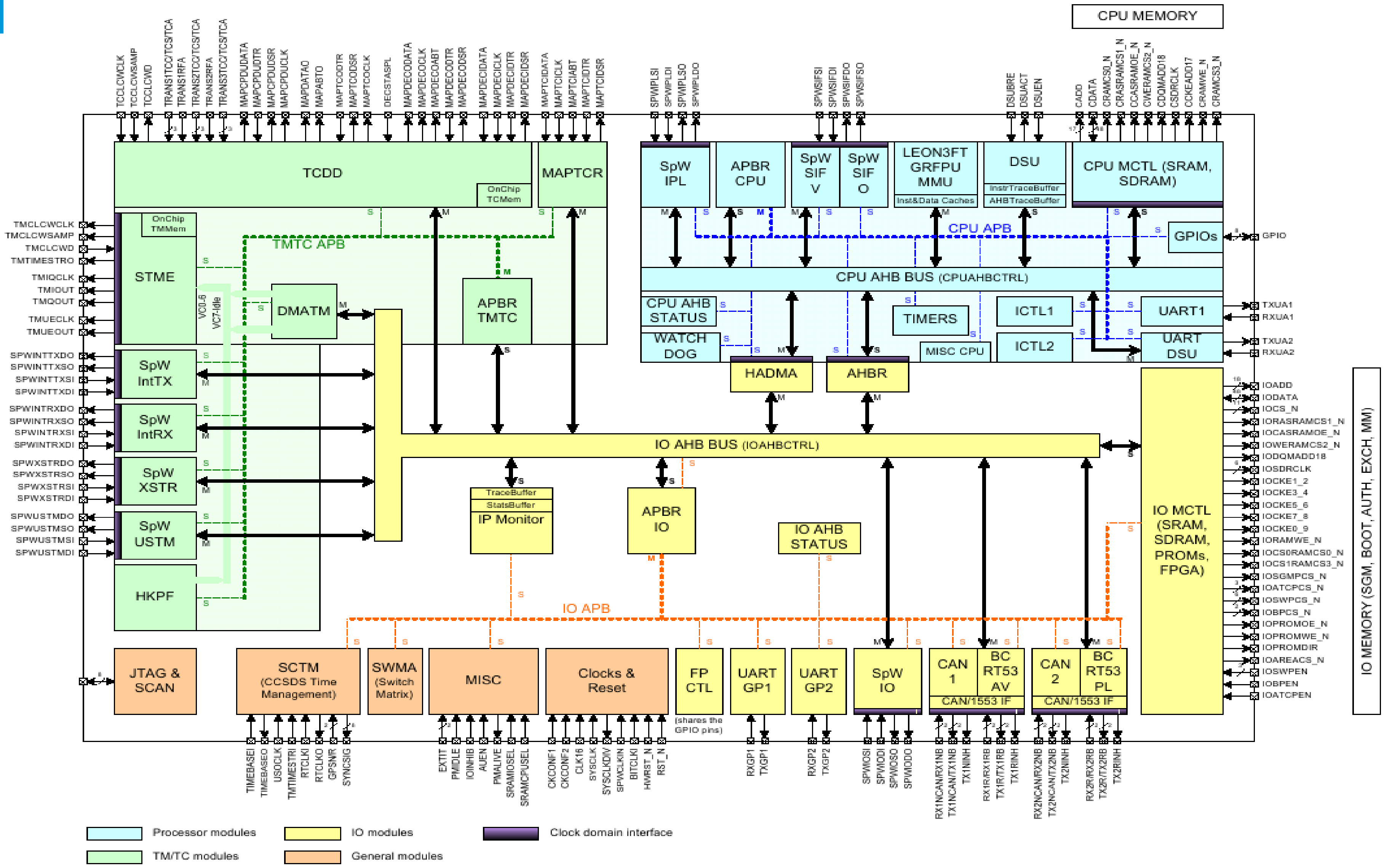
Designed by: EADS Astrium (F)
Function: payload or platform computer with telemetry and telecommand
Flying in: **SPOT6, Ingenio, Astroterra, Sentinel5p, …**

LEON3FT based Microprocessor – SCOC3

- Spacecraft Controller On-a Chip
  http://www.scoc3.com
  - LEON3FT @ 80 MHz, GRFPU
  - CCSDS TM/TC interface with X-strapping interface
  - SpaceWire, 1553, CAN, UART
  - Dual AMBA-AHB bus architecture
  - Dual PROM/SRAM/SDRAM interface
  - Basic SW development (BSP/drivers)
    SW tools (simulator, IDE) available
  - standard component, commercialised by Astrium F
  - FPGA-based Evaluation board (STARKIT)
    developed under CNES contract
  - First missions: SEOSAT, ASTROTERRA (SPOT 6/7)
    CSO (**3 French military satellites**), KRS (Kazakhstan)
  - Atmel 180 nm (1.8 Mgates + 2.2 Mbit memory)
  - Package: LGA472 with 6-sigma columns (currently assembled in the US, to be transferred to Europe)



LEON3FT based Microprocessor – SCOC3



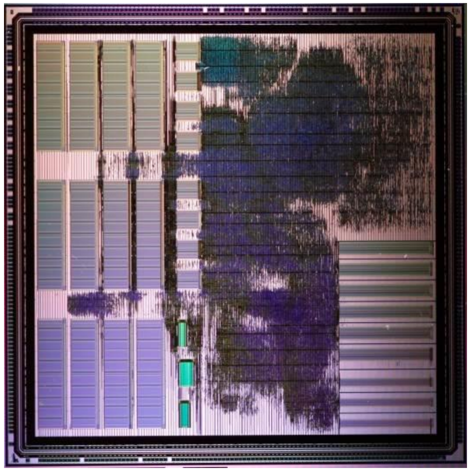
E3 run: 2010

SOLARES

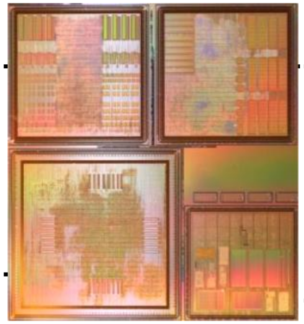
Designed by: Thales Alenia Space (E)
Function: Digital Video Broadcast - S2 packet switching
Flying in: SmallGEO

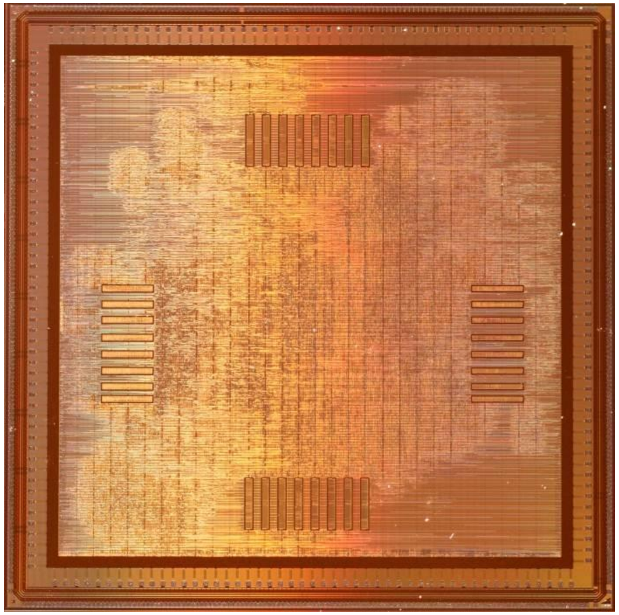
CORCONTE

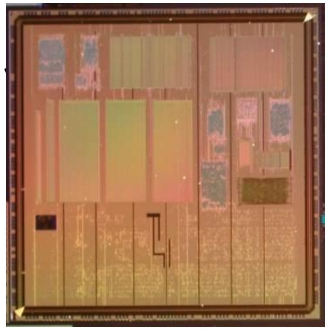
Designed by: Thales Alenia Space (E)
Function: Digital Video Broadcast-S2 encoder modulator
Flying in: SmallGEO



wafer “**reticule**”
(replicated 42 times
inside every wafer)







V40

Designed by: Atmel(F)
Function: Test Vehicle

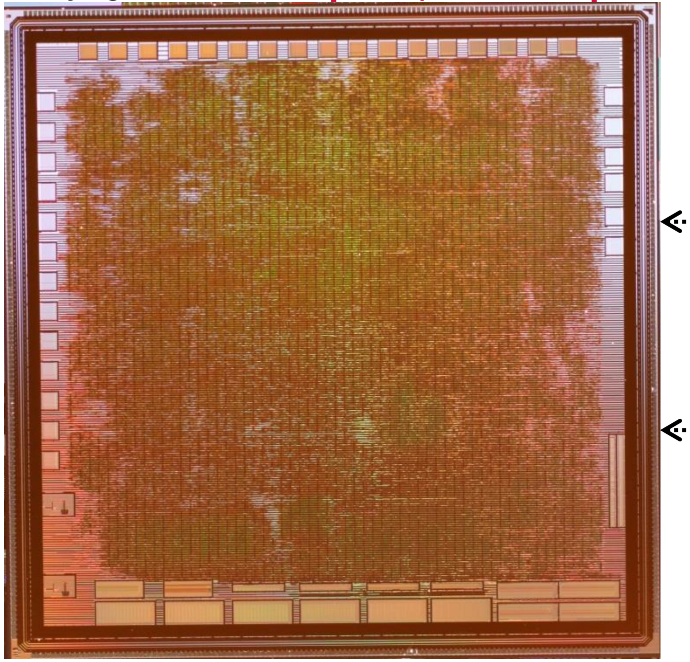
FFTC (Fast Fourier Transfer Coprocessor)

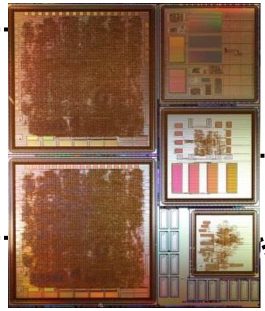
Designed by: EADS Astrium (D) + Eonic (NL)
Function: Fast Fourier Transfer Coprocessor
Flying in: Metop Second Generation

E4 run: 2011

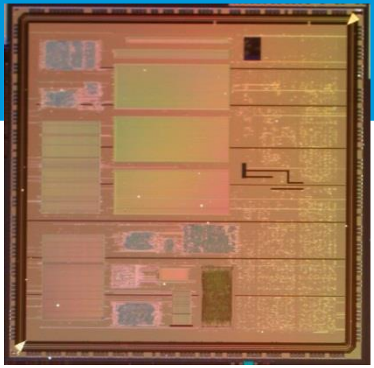
AGGA4 (Advanced GPS Galileo ASIC)

Designed by: Astrium (D)
Function: GPS Galileo GLONASS processor
Flying in: **MetOp-SG, Earth Explorer**



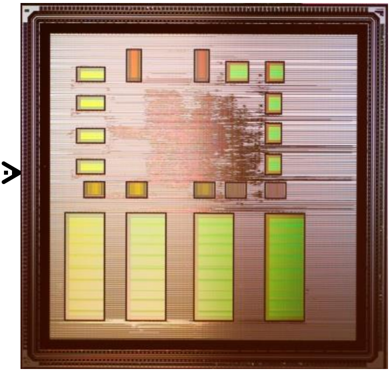


wafer “**reticule**”
(replicated 42 times
inside every wafer)



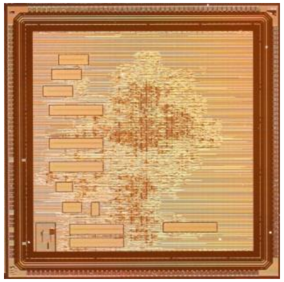
V40

Designed by: Atmel(F)
Function: Test Vehicle



APSSS

Designed by: Jena Optronik (A)
Function: Star Tracker control
Flying in: **Alphasat, Sentinel-2, Earthcare, SmallGEO, EDRS**



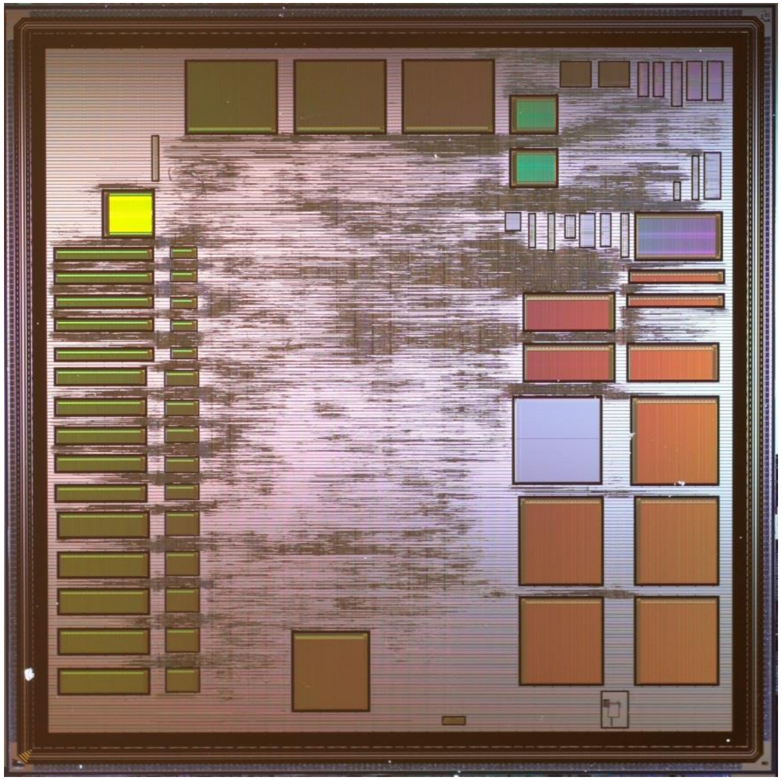
STAPLETON

Designed by: SEA (UK) + Garfield (UK)
Function: MEMS gyroscope control
Flying in: **MTG** (TBC), **Sentinel-3**

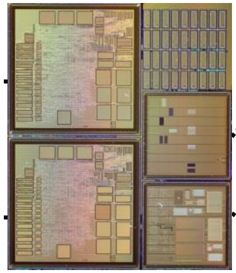
E5 run: 2012

CWICOM (CCSDS Wavelet Image Compression)

Designed by: Astrium (F)
Function: CCSDS Wavelet Image Compression
Flying in: **Sentinel-2b** (TBC)

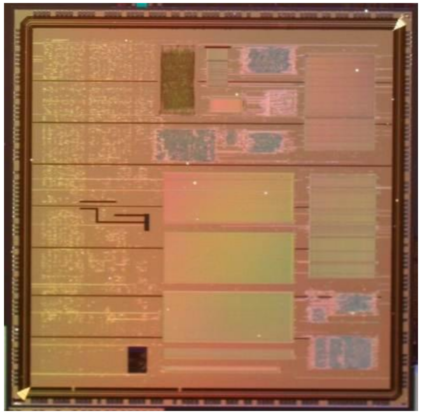


wafer “**reticule**”
(replicated 35 times
inside every wafer)



V47

Designed by: Atmel(F)
Function: Test Vehicles



V40

Designed by: Atmel(F)
Function: Test Vehicle

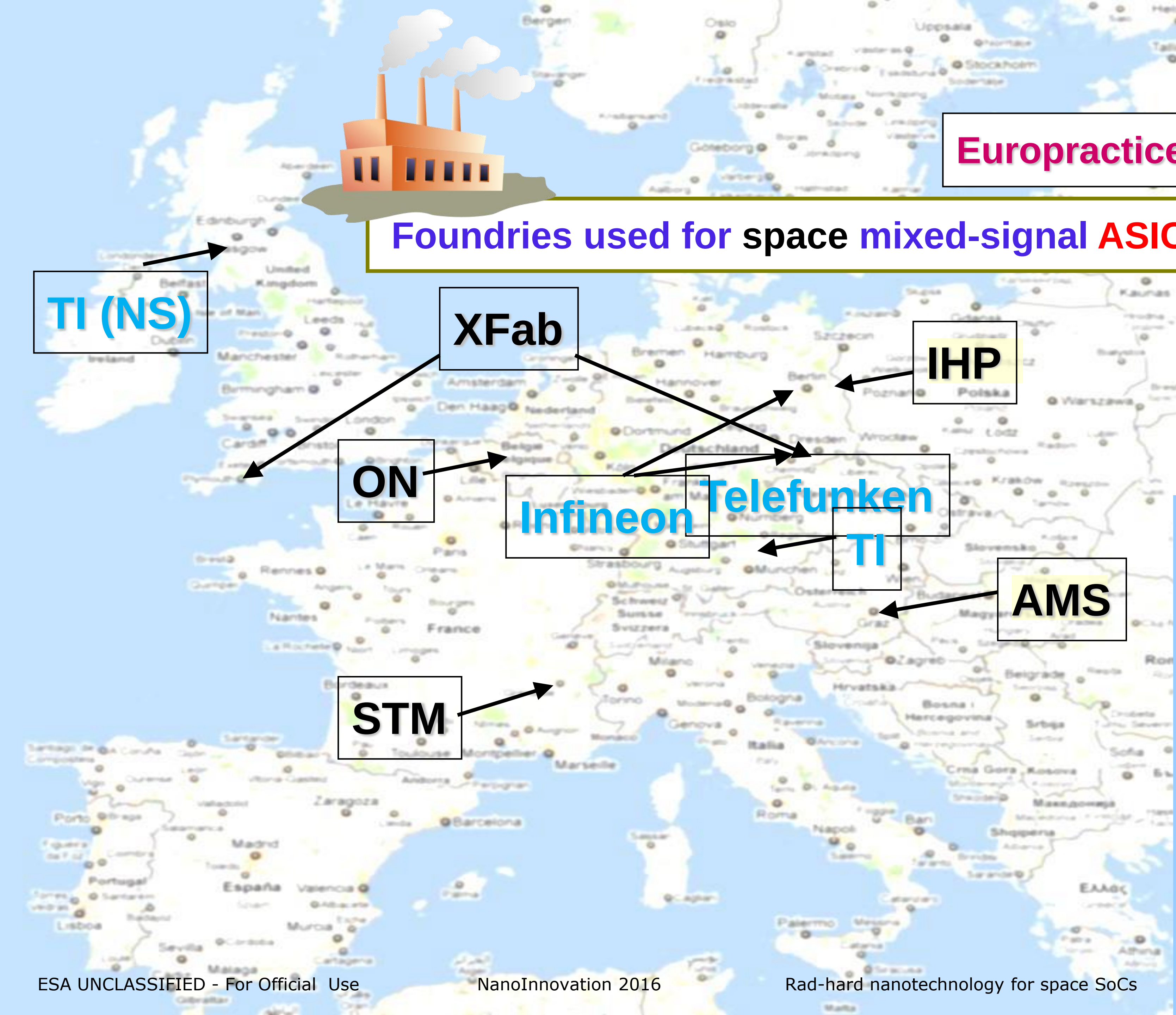
Space Multi Project Wafer (MPW) programme

- TRP
- 2.3M€
- Atmel(F)

Space Multi Project Wafer programme: **accomplishments**

- **9** years
- **6** manufacturing runs (more outside this contract)
- **150** silicon wafers
- **14** different ASIC designs
- **11** companies
- **> 17** satellites use/will use these ASICs

Foundries used for space mixed-signal ASICs



Europractice + CMP

TI (NS)

XFab

IHP

ON

Infineon

Telefunken

TI

AMS

STM

Corea

Magna
Chip

Taiwan

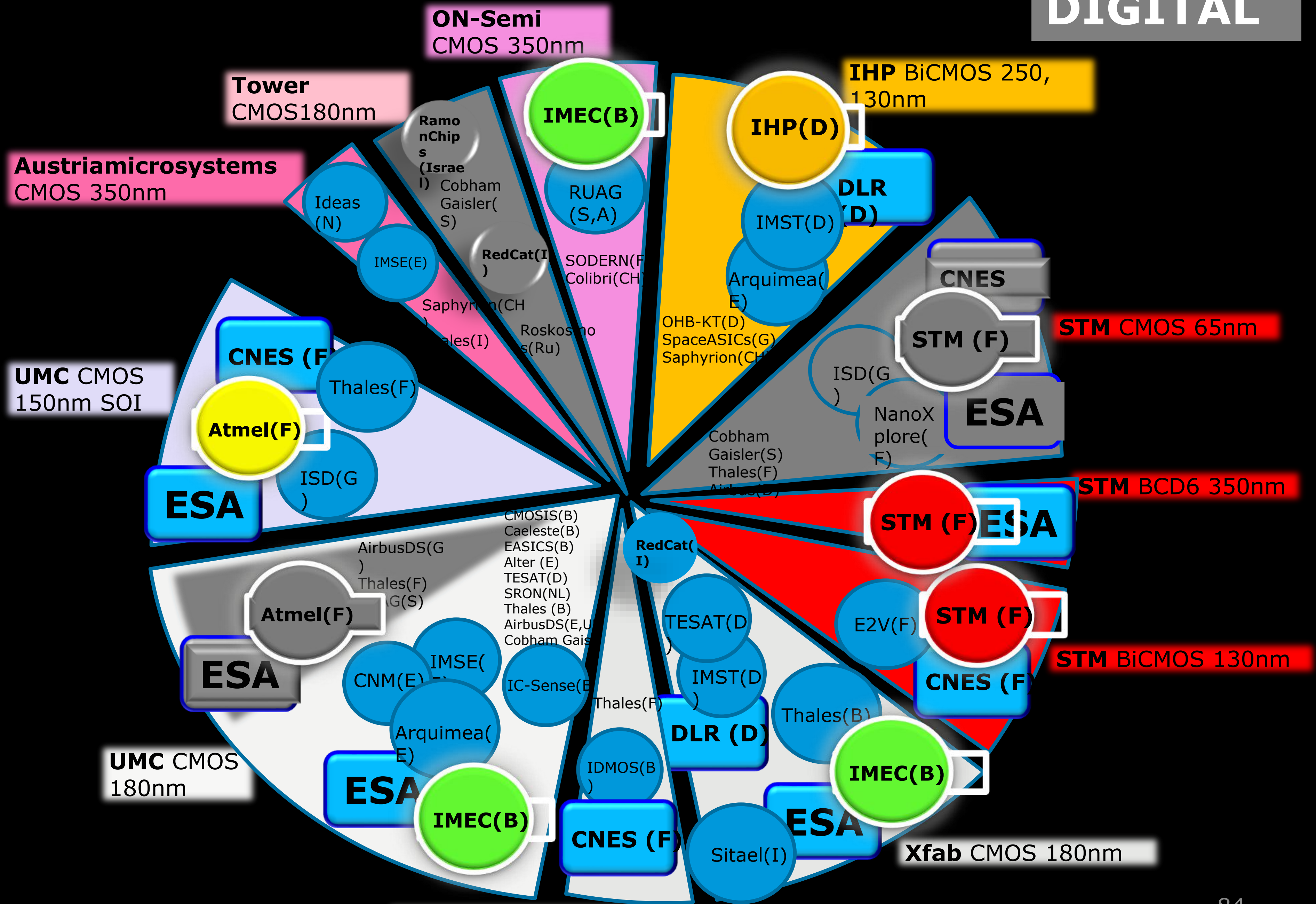
UMC
TSMC

Israel

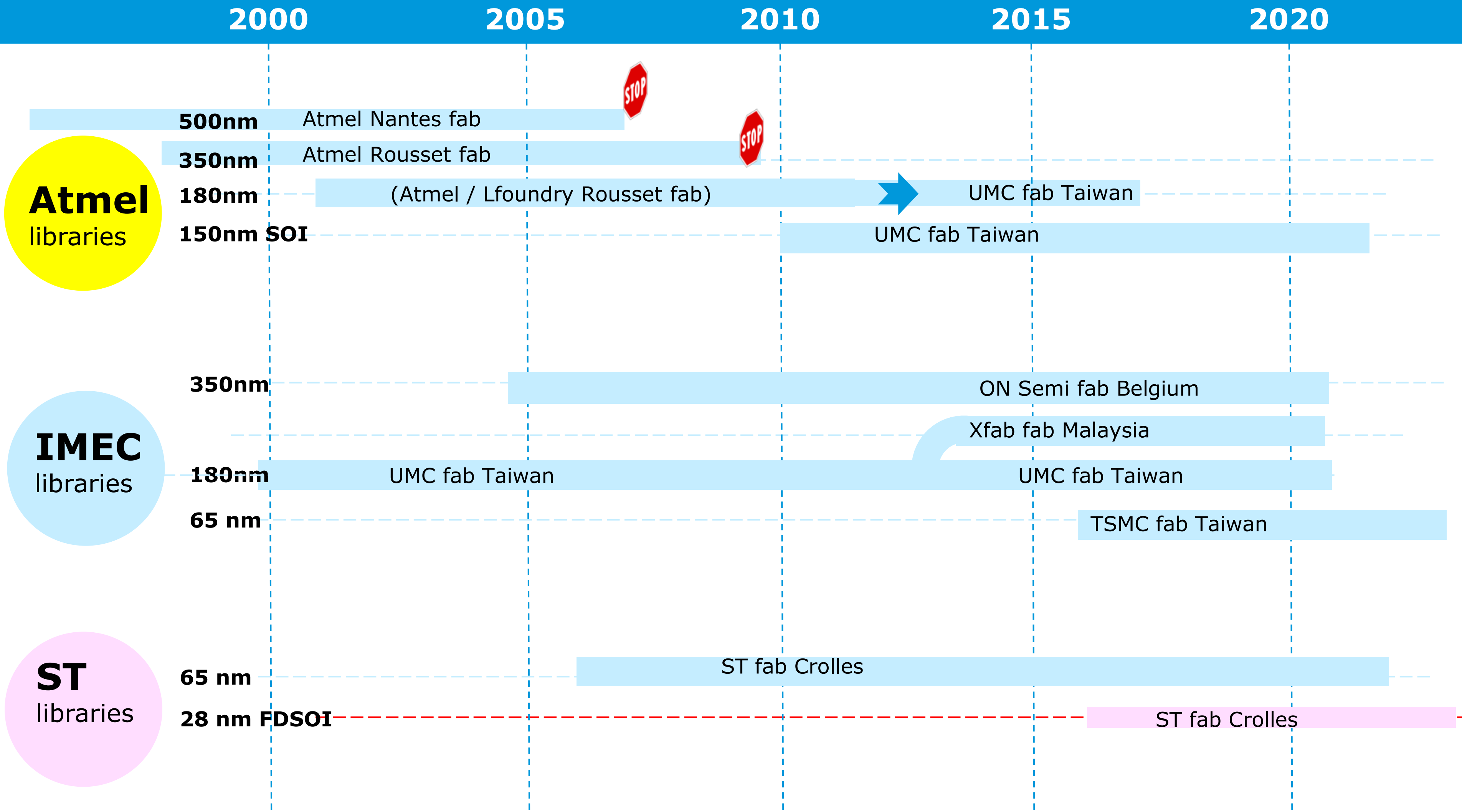
Tower

Space ASIC Technology Observatory (Jan 13th 2016)

DIGITAL

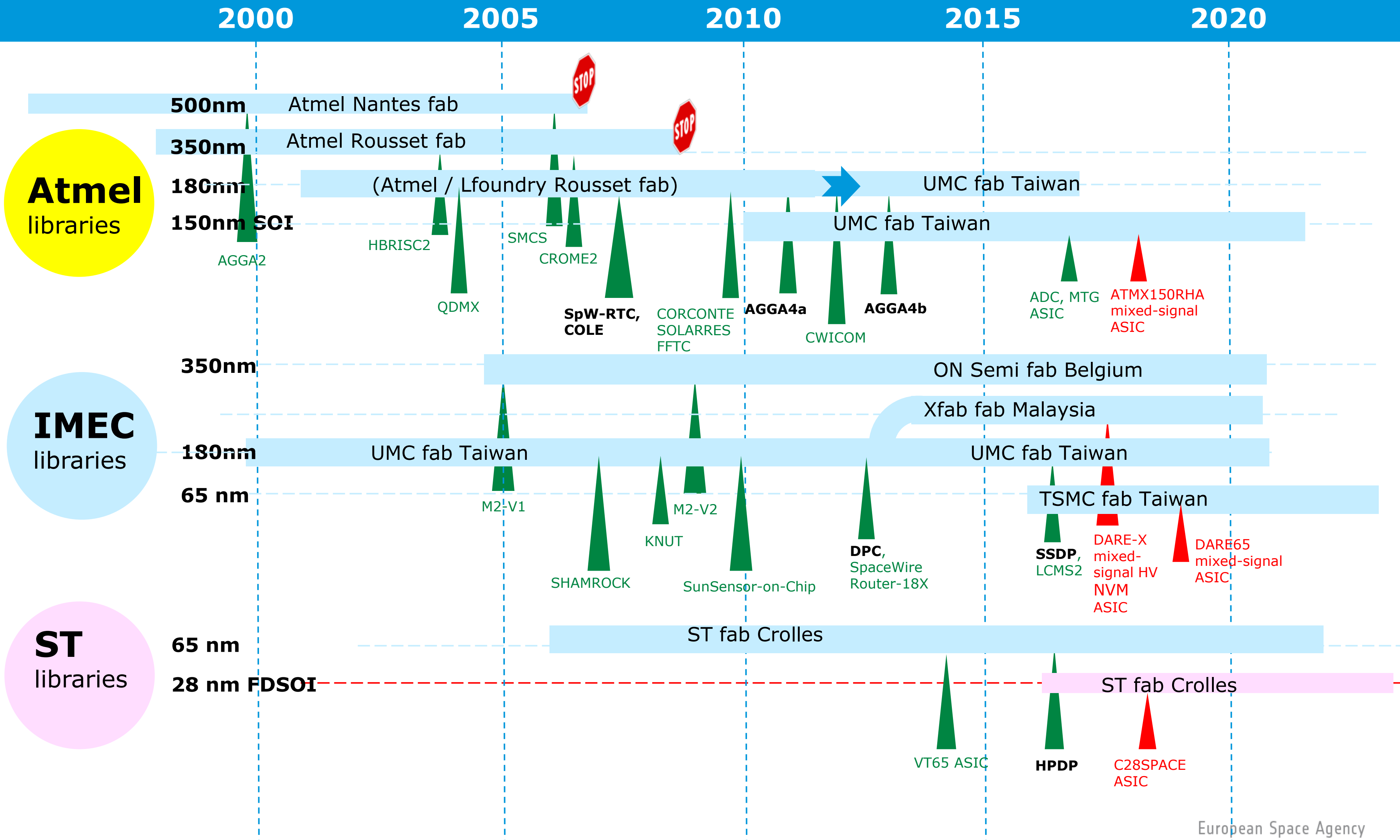


European Deep Sub-Micron (DSM) processes & libraries for space microchips



Other processes: IHP 250, 130nm, ST 350, 130nm, Infineon AMS 350nm, Xfab 350nm, (Lfoundry 150nm SOI under evaluation)

European DSM processes & libraries for space ASICs (digital, mixed-signal, many embed microprocessor , DSP cores…)



2000
2005
2010
2015
2020

Atmel libraries

500nm Atmel Nantes fab
350nm Atmel Rousset fab
180nm (Atmel / Lfoundry Rousset fab) UMC fab Taiwan
150nm SOI UMC fab Taiwan

AGGA2
HBRISC2
QDMX
SMCS
CROME2
SpW-RTC, COLE
CORCONTE
SOLARRES
FFTC
AGGA4a
CWICOM
AGGA4b
ADC, MTG ASIC
ATMX150RHA mixed-signal ASIC

IMEC libraries

350nm ON Semi fab Belgium
Xfab fab Malaysia
180nm UMC fab Taiwan UMC fab Taiwan
65 nm TSMC fab Taiwan

M2-V1
SHAMROCK
KNUT
M2-V2
SunSensor-on-Chip
DPC, SpaceWire Router-18X
SSDP, LCMS2
DARE-X mixed-signal HV NVM ASIC
DARE65 mixed-signal ASIC

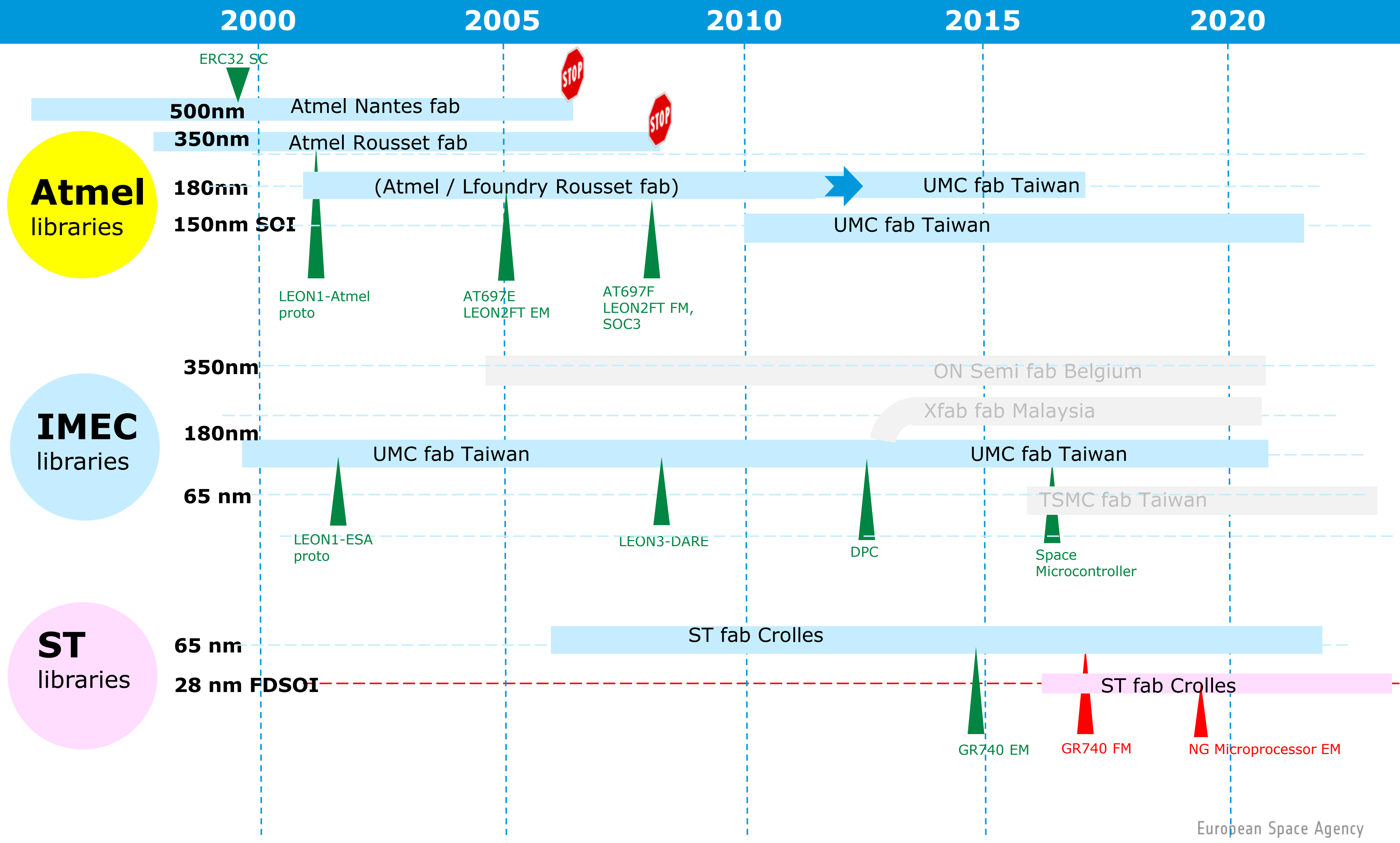
ST libraries

65 nm ST fab Crolles
28 nm FDSOI ST fab Crolles

VT65 ASIC
HPDP
C28SPACE ASIC

European Space Agency

European DSM processes & libraries for space **Microprocessors**



2000
2005
2010
2015
2020

Atmel libraries

500nm Atmel Nantes fab

350nm Atmel Rousset fab

180nm (Atmel / Lfoundry Rousset fab) UMC fab Taiwan

150nm SOI UMC fab Taiwan

ERC32 SC

LEON1-Atmel proto

AT697E LEON2FT EM

AT697F LEON2FT FM, SOC3

IMEC libraries

350nm ON Semi fab Belgium

Xfab fab Malaysia

180nm UMC fab Taiwan UMC fab Taiwan

65 nm TSMC fab Taiwan

LEON1-ESA proto

LEON3-DARE

DPC

Space Microcontroller

ST libraries

65 nm ST fab Crolles

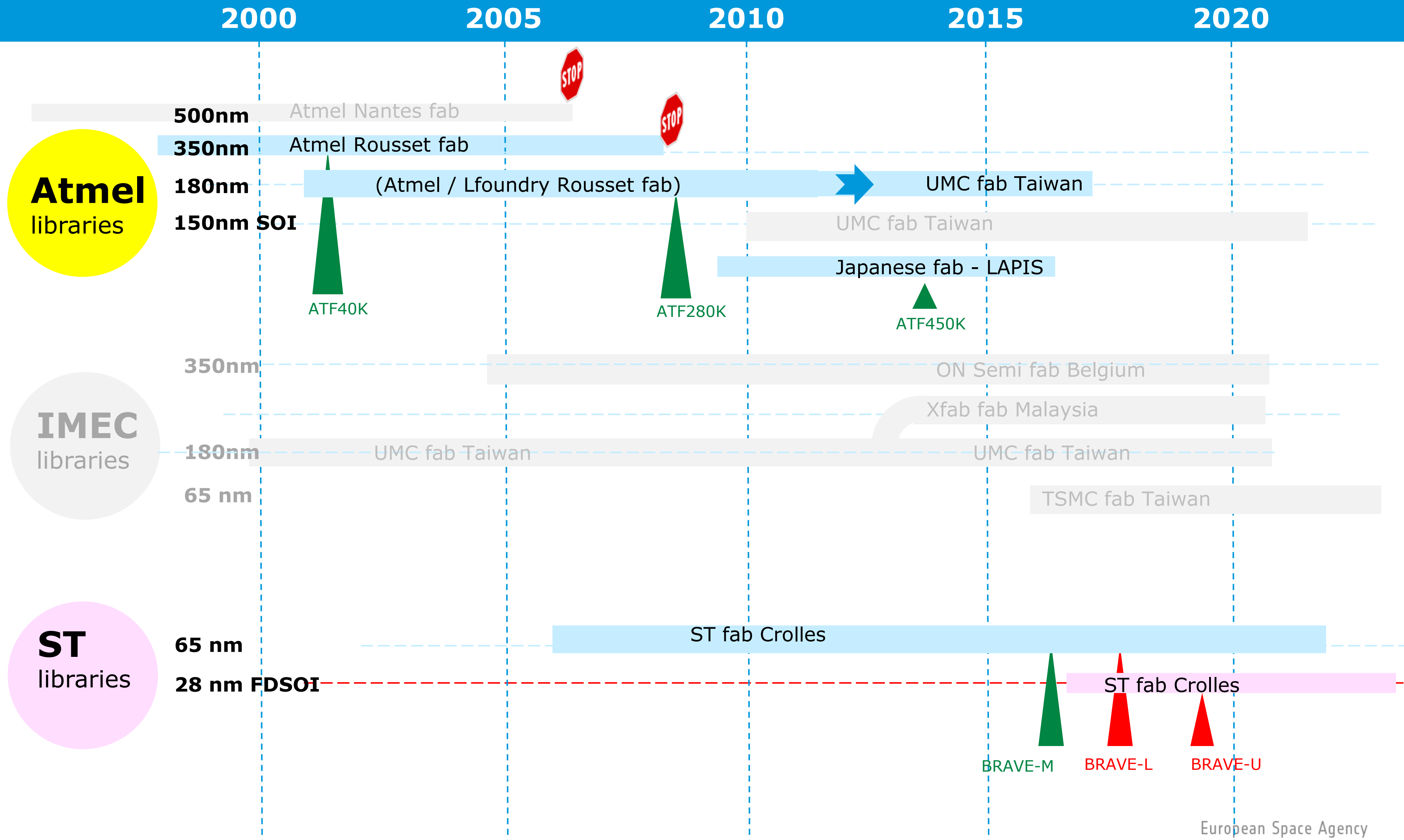
28 nm FDSOI ST fab Crolles

GR740 EM

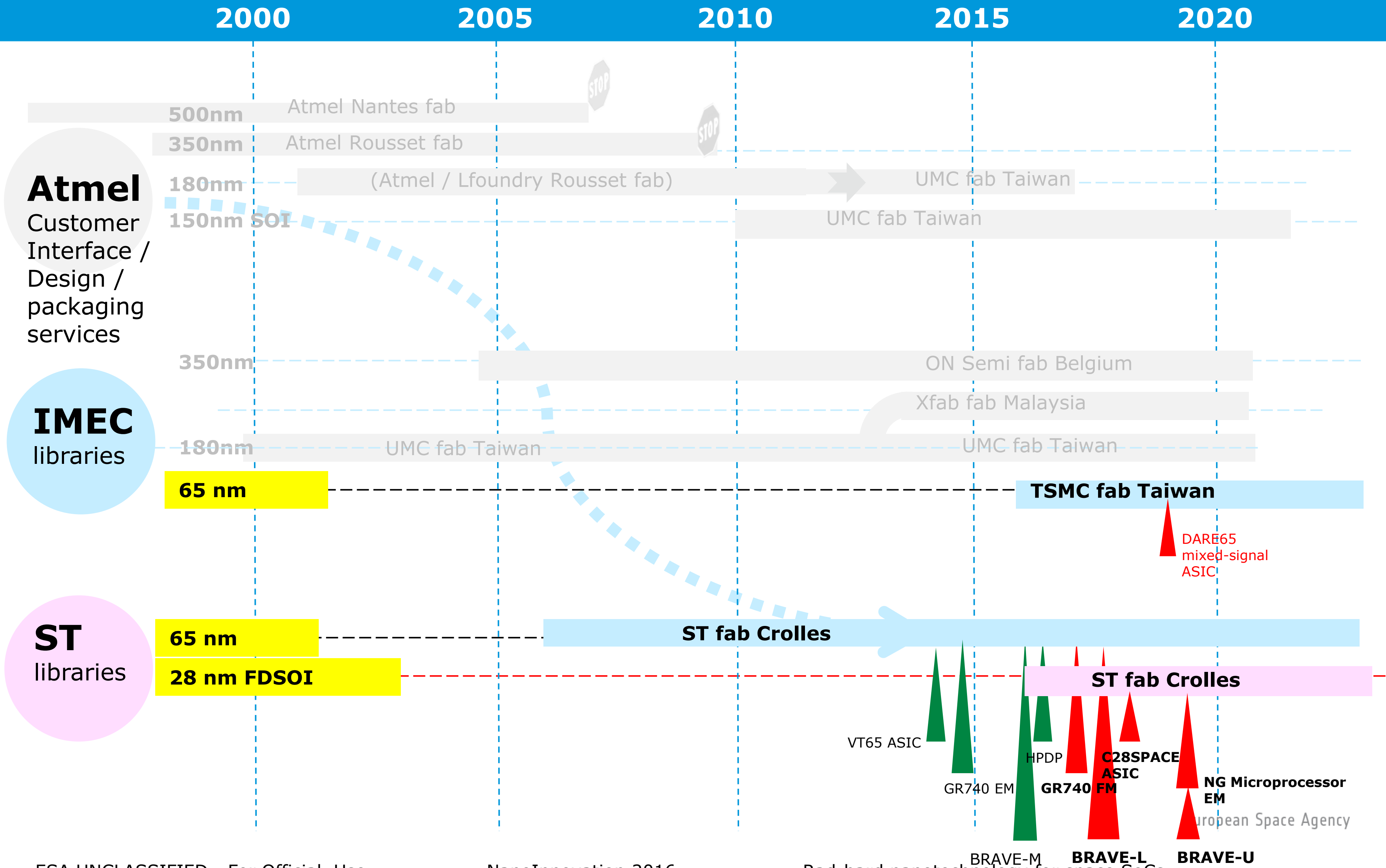
GR740 FM

NG Microprocessor EM

European DSM processes & libraries for space **FPGAs**



European DSM processes & libraries for space microchips: 65nm and below



2000 2005 2010 2015 2020

Atmel
Customer Interface / Design / packaging services

500nm Atmel Nantes fab

350nm Atmel Rousset fab

180nm (Atmel / Lfoundry Rousset fab) UMC fab Taiwan

150nm SOI UMC fab Taiwan

IMEC
libraries

350nm ON Semi fab Belgium

Xfab fab Malaysia

180nm UMC fab Taiwan UMC fab Taiwan

65 nm **TSMC fab Taiwan**

DARE65 mixed-signal ASIC

ST
libraries

65 nm **ST fab Crolles**

28 nm FDSOI **ST fab Crolles**

VT65 ASIC

GR740 EM

BRAVE-M

HPDP

GR740 FM

BRAVE-L

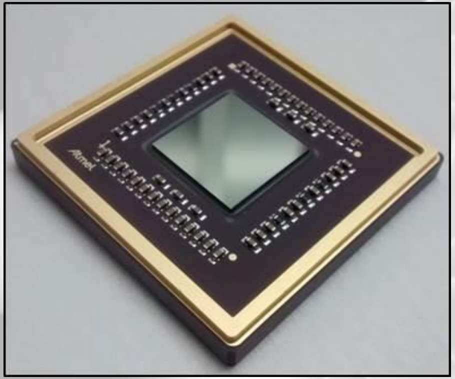
C28SPACE ASIC

NG Microprocessor EM

BRAVE-U

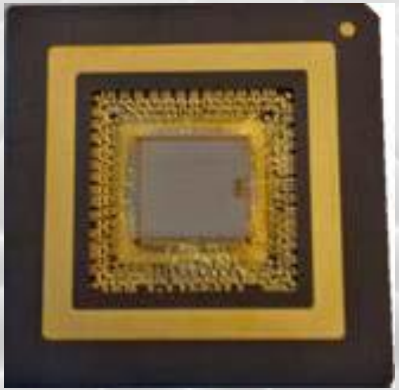
State of the art , most recent European deep submicron microchips

2015



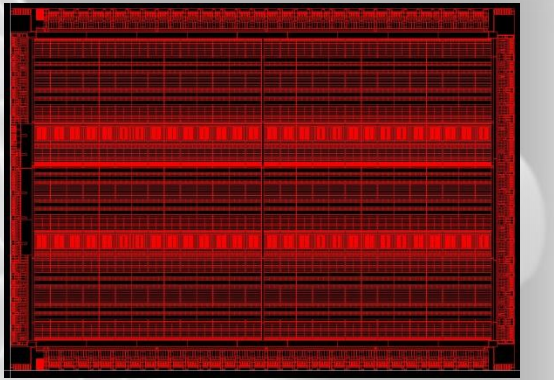
“**VT65**”
Telecom payload
processor
200 mm²
1752 pins
TAS/ST/Atmel/E2V/CNES

2015



“**NGMP**/GR740”
General Purpose Microprocessor
70 mm²
625 pins
Cobham Gaisler/ST/E2V/ESA

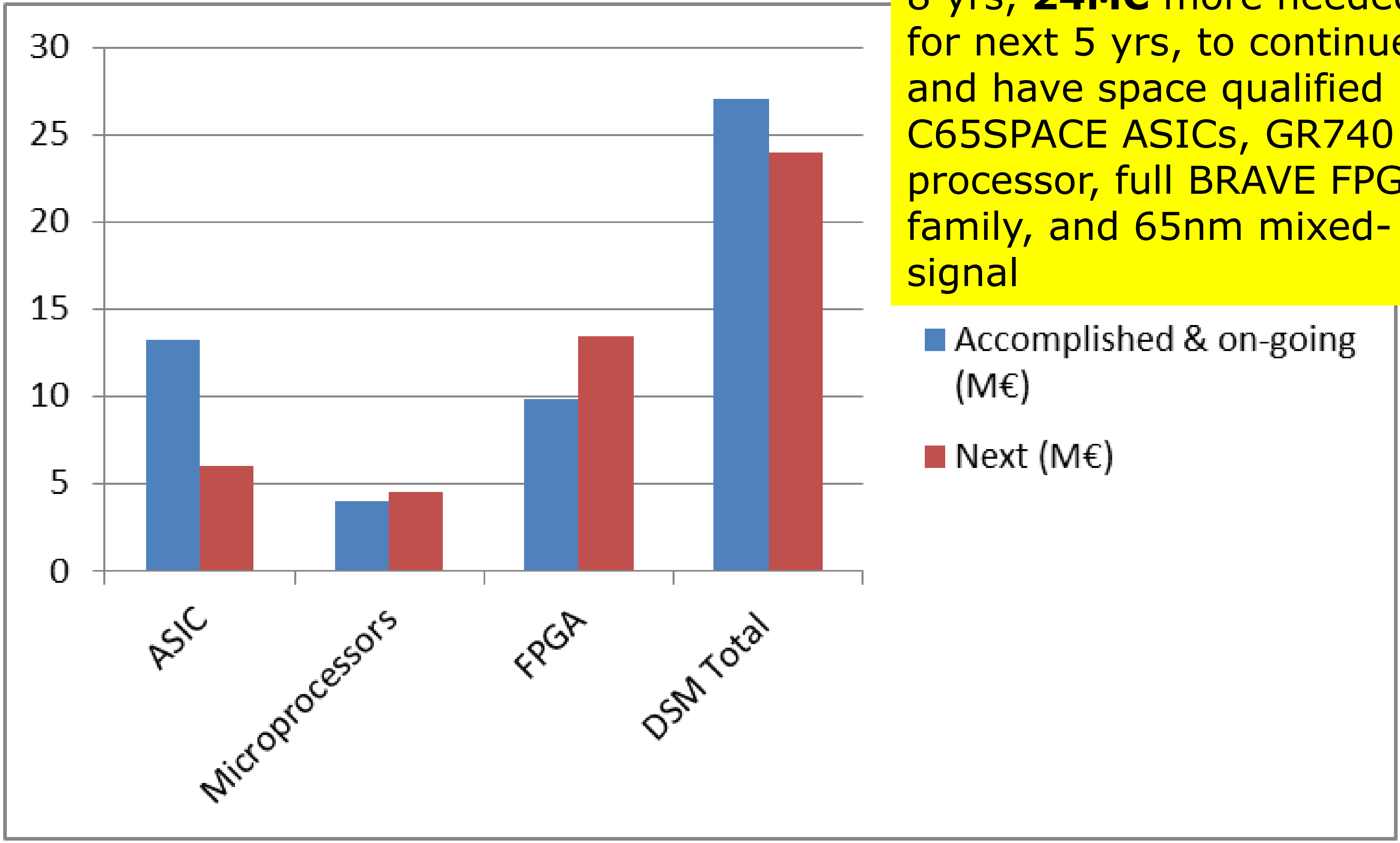
2016



“**BRAVE** FPGA”
General Purpose
Reprogrammable
70 mm²
625 pins
NanoXplore/ST/E2V/ESA

All manufactured with 65nm rad-hard microchip technology provided by STMicroelectronics & partners

Space Deep Submicron achievements, next steps



About **26M€** spent in past 8 yrs, **24M€** more needed for next 5 yrs, to continue and have space qualified C65SPACE ASICs, GR740 processor, full BRAVE FPGA family, and 65nm mixed-signal

Agency

Space Microelectronics Roadmaps Challenges

- **DSM 65nm** ASIC offer (+ high-end packaging). Conclude the space qualification, and make the Design Kit accessible
- **Next Generation (and European!)** generic purpose ICs: GR740 Microprocessor, NG-DSP, Microcontroller, reprogrammable FPGA family (BRAVE-MEDIUM, LARGE, ULTRA)
- **Consolidate mixed-signal** ASIC offer (end-to-end quality, costs, HV, NVM, HT, HF…), including 65nm node
- **Fragmentation of ASIC supply chain**: more difficult & expensive to guaranty space quality (vs. one-stop-shop vendor)
- **Analogue IP Cores**, re-use, IPR and support solutions
- All of the above: **space qualified & sustainable**

THANKS for your attention!

QUESTIONS ?

More information in

European Space Technology Harmonisation Technical Dossier

MICROELECTRONICS:

ASIC and FPGA

Currently following the harmonisation exercise, to be released Q1 2017

http://www.esa.int/TEC/Microelectronics/